IVS Technology Development Center at Haystack Observatory

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Abstract

Recent and planned activities of the IVS Technology Development Center at Haystack Observatory are reviewed, with an emphasis on the Mark IV correlator, Mark IV decoder, and thin-film head array projects.

1. Mark IV Correlator

Introduction

The Mark IV correlator development at Haystack Observatory is nearing completion. Copies of this correlator will soon be in place at USNO in Washington, D.C., MPI/Bonn in Germany, and MIT Haystack Observatory in Westford, Massachusetts. A nearly identical copy is in operation at JIVE in Dwingeloo, The Netherlands. Development of the Mark IV VLBI correlator system is a joint U.S.-European effort, with sponsorship by NASA, USNO, and the Smithsonian Institution in the U.S., and BKG, JIVE, and NFRA in Europe. Two large correlators for connected-element interferometers, in Westerbork, The Netherlands and on Mauna Kea, Hawaii, are also based on the same correlation engine as the Mark IV correlators.

In the intial implementation the USNO, MPI, and Haystack correlators will all support $\sim$8 stations, though the architecture allows easy future expansion to many more stations.

Features of the Mark IV Correlator

The Mark IV correlator system is designed as a major upgrade of the venerable Mark IIIA correlator, which has been in use since 1985 at Haystack, USNO, and MPI/Bonn. The characteristics of the Mark IV correlator can be summarized as follows:

- 1 Gbit/sec/station playback rate, expandable to 2 Gbits/sec/station
- Scalable architecture allowing up to 32 stations with 16 channels/station, all baselines correlated simultaneously
- Compatibility with Mark IIIA, Mark IV and VLBA format tapes
- Station-based XF architecture utilizing full-custom VLSI correlator chips
- 4$\times$ playback speedup compared to Mark IIIA correlator
- Extensive use of VEX files for correlator operation/configuration
- Updated HOPS post-correlation package

Architectural Overview

Figure 1 shows a simplified block diagram of a 16-station, 1 Gbit/sec/station Mark IV correlator. Each Playback Unit (PBU) is attached to a Station Crate which reconstructs the data from the tape into channels and then applies the proper computer model to the delay and delay rate of the data. The delay, delay rate, and phase models for each channel of each station are periodically

inserted into the data streams transmitted to the Correlator Crate. In order to minimize cabling complexity between the Station Crates and the Correlator Crate, the transmission between them takes place over high-speed serial links on coax cable.

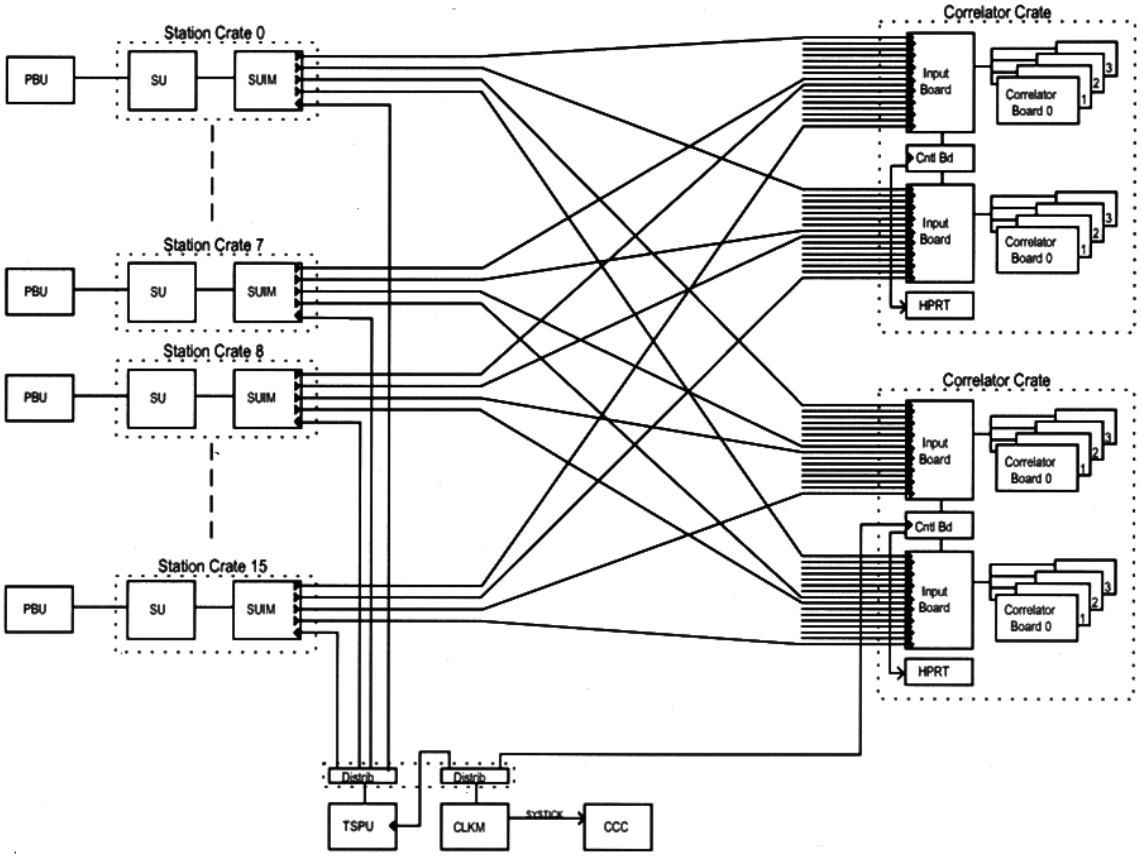

Figure 1. Block diagram of Mark IV correlator.

At the Correlator Crate the data are resychronized and passed to the Correlator Board where the station parameters are captured and are used to compute the baseline processing parameters supplied to the correlator chips. The lag-correlation results are periodically read from the correlator chips and passed to the Correlator Control Computer (CCC) for further processing.

Correlator Chip and Board

Haystack Observatory was responsible for the development of the correlation engine, which includes a full-custom VLSI correlator chip and the correlator board which hosts the correlator chips. Approximately 10,000 chips were fabricated by Hewlett-Packard. The characteristics of the correlator chip are as follows:

- Full-custom CMOS with ~1,000,000 transistors
- 1 or 2 bits/sample
- 64 MHz clock rate

- 512 lags which can be re-arranged internally into several independent correlator sections, each having from 16 to 512 lags
- 8 internal 32-bit phase generators and rotators for rotation rates to full channel bandwidth
- internal bit-shift/phase-shift algorithm
- internal vernier-delay management
- 24-bit latchable ripple counter on each lag
- Power dissipation: ∼3W at 64 MHz
- 208-pin PGA package, ∼2 inches square

Figure 2 shows a single correlator board. Each correlator board, which is approximately 40 cm by 50 cm in size, hosts 32 correlator chips, two high-speed DSP chips, and 10 64x64 custom ASIC crossbar switches. The characteristics of a correlator board are as follows:

- 32 VLSI correlator chips
- access to 64 2-bit data streams configurable through 10 64x64 custom ASIC cross-bar switches
- 64 MHz maximum clock rate (tested to 70 MHz)
- 16,384 real lags per board, flexibly configurable
- support of 128 baselines of 32 complex lags per baseline for a single channel
- auto-correlation modes

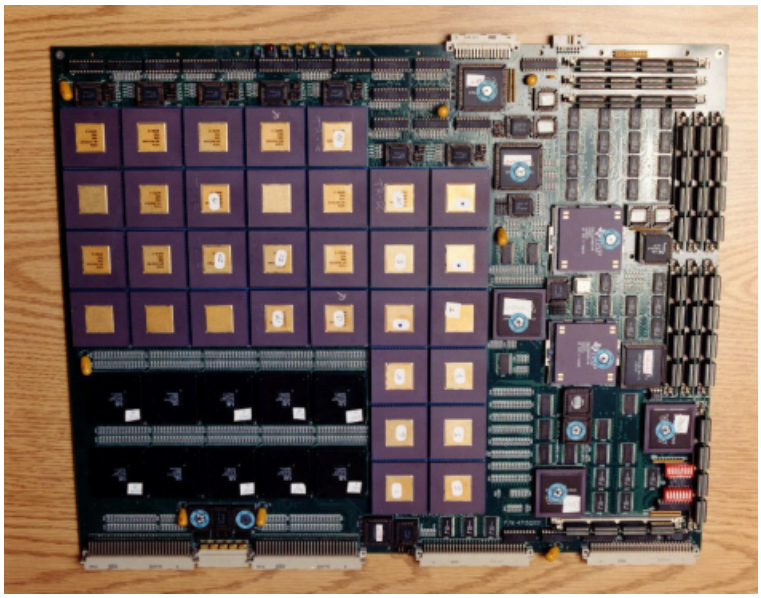

Figure 2. Mark IV correlator board.

Each correlator crate houses eight correlator boards. Two such crates are necessary for a full 16-station, 1-Gbit/sec/station correlator.

Status and Plans

All Mark IV correlator hardware has been constructed, and software development is in the final stages, with deliveries of operational correlators to USNO and MPI/Bonn expected in late summer or early fall of 1999. Figure 3 shows a diagram of the final configuration with 8 playback units. The correlator rack is in the center, and each Station Crate is surrounded by the four playback units it serves. The Mark IV correlators will replace the Mark IIIA correlators now currently in use at these locations.

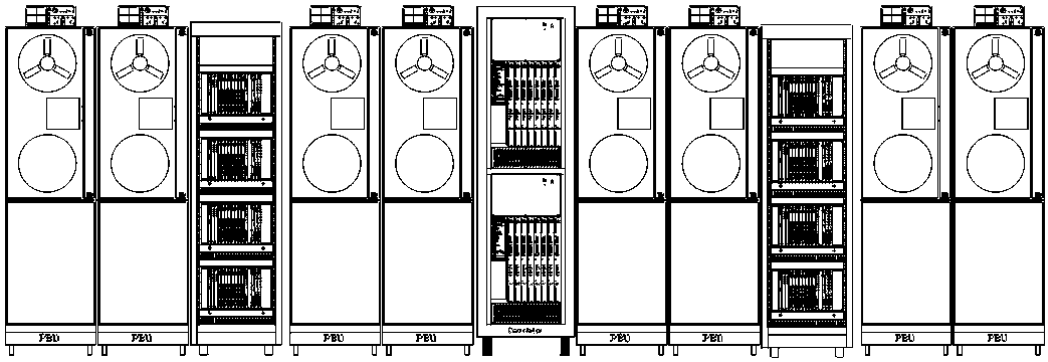

Figure 3. Mark IV correlator configuration with eight playback units.

2. Mark IV Decoder

The Mark IV decoder module is designed as a plug-in upgrade/replacement for the Mark III decoder. As a direct replacement, it acts as a two-channel data-quality analyzer operating the same way as the Mark III decoder, that is, it accepts two tape-tracks of data from either the formatter or from the playback-monitor tracks on the recorder. However, it can operate at up to the full 18 Mbps rate of the Mark IV formatter.

In addition, the Mark IV decoder accepts four selectable channels of 2 bits/sample data from the Mark IV formatter via a separate connector on the rear panel. These data can be analyzed by an internal Mark IV correlator chip to simultaneously extract up to four arbitrarily placed phase-cal tones from any of the four selected channels, or the correlator chip may act as a state counter for a single selected channel. Future plans include the ability of the correlator chip to also extract high-resolution bandpass information from any or all of the selected Mark IV formatter channels.

The Mark IV decoder utilizes a Motorola 68340 processor with 64 MB of internal RAM, of which about 60 MB is available for data capture, either from one playback track or from one Mark IV formatter channel. The data may then be read out from the decoder either through the standard MAT bus or via a separate high-speed SCSI connection.

Production of a number of Mark IV decoders is now proceeding at Haystack Observatory. The design will soon be transferred to industry and made available to interested parties.

3. Thin-Film Head Array Project

Haystack Observatory is working with industry, with support from NASA, NRAO and JIVE, to develop thin-film (TF) head array technology suitable for use with VLBI. In particular, the goal of the project is to develop a thin-film array replacement for the current headstacks used in the Mark IV/VLBA recording systems.

Thin-film head technology utilizes semi-conductor fabrication techniques to construct read/write heads. Write heads are created by constructing thin-film coils which drive a magnetic gap in the conventional manner. Read heads utilize magneto-resistive technology (MR) which is increasingly prevalent in the hard disc industry. These read/write head pairs are deposited in arrays along a 1-inch substrate bar; standard wire-bonding techniques are used to attached flexible printed-circuit assemblies to the bar for access by the external world.

Haystack has received and tested several prototype TF/MR headarrays and has found excellent performance under a wide variety of tape speeds and tensions using an innovative "flat-lap" contour invented at Haystack. This "flat-lap" contour has been extensively analyzed, both theoretically and experimentally, and is now understood to actually create a suction of the tape to the head in such a way as to always maintain excellent head-to-tape contact.

In addition to excellent performance, the TF/MR headarrays show practically no wear after thousands of hours of operation; this is due to the extremely hard substrate material used in their manufacture.

Haystack Observatory is now exploring with industry ways in which these TF/MR headarrays can be replicated in a cost effective way. Our goal is to be able to manufacture a complete headarray assembly for a price substantially less than a conventional headstack. Negotiations with industry in this regard are now underway. A new design for the read/write electronics will be required to support the TF/MR headarrays. Work on these components will accelerate once the availability of the headarrays is assured.

4. Mark IV Acquisition Systems

To help stations that currently have either Mark IIIA or VLBA data acquisition systems convert to Mark IV, we are providing assistance through acquisition of hardware, installation of the new hardware at the stations, and training the local staff in its use. In the past year we helped upgrade the systems at Hartebeesthoek and Wettzell, and in the coming year we will upgrade Matera and O'Higgins.

5. Personnel

The Haystack Observatory scientists, engineers, and technicians who have contributed to the work described in this report are Will Aldrich, John Ball, Ed Beauchemin, Tom Buretta, Peter Bolis, Roger Cappallo, Kevin Dudevoir, David Fields, Roger Genereux, Joel Goodman, Hans Hinteregger, Colin Lonsdale, Sinan Müftü, Ed Nesman, Arthur Niell, Alan Rogers, Stu Sherman, Dan Smythe, Alan Whitney, and Ken Wilson.