IAA Technology Development Center Report for 2017–2018

Evgeny Nosov, Evgeny Khvostov, Alexander Vytnov

Abstract In 2018, the IAA finished the construction of a new 13-meter radio telescope (RT-13) at the Svetloe observatory. The main activity of the IAA Technology Development Center was focused on equipping the new antenna with a VGOS-compatible signal chain and a clock and frequency distribution system. The presented report briefly gives an overview of this activity.

1 General Information

In 2015 two multi-band, fast rotating antennas with a mirror diameter of about 13.2-m (RT-13) were installed at the Zelenchukskaya and Badary stations [1]. The inaugural ceremony of the third RT-13 radio telescope at the Svetloe observatory was held on September 19, 2018. Each RT-13 radio telescope is equipped with a specially designed receiver system. The main feature of this system is the cryogenic receiver unit that includes a cooled tri-band feed and low-noise amplifier. Such a design makes it possible to achieve high sensitivity and to receive weak noise signals of cosmic origin. As well, the feed design allows us to receive signals in three frequency bands: S (2.2—2.6 GHz), X (7.0—9.5 GHz), and Ka (28—34 GHz) in both circular polarizations simultaneously [2].

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2 Wideband Receiver

The UWB (ultra-wideband) receiving system designed in the IAA RAS is purposed for implementation at the “Quasar” VLBI Network RT-13 radio telescopes [3]. The UWB receiving system operates in 3–16 GHz band on dual linear orthogonal polarizations. It is fully compatible with RT-13 mechanical, cryogenic, and electric interfaces. It is supposed that the UWB system can replace the Tri-band system and be replaced by it on demand.

The UWB system operates the following way. The radiation from a source, focused by the dish and the subreflector, comes through the radio-transparent cover of the cryo unit to the focal center of the QRFH feed, where it is separated into vertical and horizontal linear polarizations. Two signals, mixed with calibration signals at the direct coupler, are amplified with cryogenic LNAs, and every signal is divided four ways by the splitter unit. The splitter unit also includes room temperature pre-amplifiers. Dual-channel FCUs use up-down conversion to select from the input range 3–16 GHz, 1 GHz band, to the BRAS system [4] bandwidth (1–2 GHz).

3 Multifunctional Digital Backend (MDBE)

The MDBE is intended for equipping all radio telescopes of the “Quasar” VLBI network with a unified, both legacy- and VGOS-compatible, digital backend. The system consists of up to 12 DPS units, connected by backplane with the Synchronization and Control Unit (Figure 1). Each DSP unit digitizes an input IF signal by using the 4096 MHz sampling frequency, performs necessary digital processing in the FPGA, and outputs the data through a 40 Gpbs or 10 Gbps fiber optical link. Table 1 presents the basic parameters of the MDBE.

Table 1 Basic parameters of MDBE.

Number of IF inputs (DSP units)	up to 12
Input frequency range	0.5–2048 MHz
Sampling frequency	4096 MHz
Synchronization	5/10/100 MHz 1 PPS (two inputs) 1 PPS monitor
Outputs per DSP unit	1x10 Gbps (SFP+) 1x40 Gbps (QSFP)
Output format	VDIF in raw Ethernet frames VDIF in UDP packets
Calibration features	PCAL extractor & analyzer Inner delay variation control Noise calibration
Control interface	10/100/1000 Ethernet (Fiber or copper)
Basic VLBI modes	Wideband channels: 2048, 1024, or 512 MHz DDCs mode: 8, 16, or 32 MHz
Size	19" 3U case + 1U fan unit

Like the previous backend, the BRAS [4], the MDBE will be located in the focal cabin of the antenna, near to the receiver. As there is no direct access to the system for the staff while observing is in progress, the MDBE provides full remote control of the system and signals. The control features include measuring voltages, currents, fan speed, and temperatures in key points of the system. Each DSP unit logs signal power, statistics of 2-bit output data, the extracted PCAL signal (in the time domain), estimation of its group delay, and phases and amplitudes of the tones. MDBE has an embedded calibration system that allows it to control the phase/delay stability of the clock synthesizer and ADCs.

Currently the design stage is finished, and the first sample of the MDBE is in production. Figure 2 presents the view of the DSP unit without a radiator and a front panel. The radiator (not shown in the figure) covers the board to effectively remove the heat produced by the FPGA, the ADC, and other parts. It also divides the board into a few partitions to shield sensitive ADC parts from a noisy digital environment. The clock generator (Figure 3), which is a part of the Synchronization and Control Unit, also has been produced and is undergoing testing.

The first field test of the MDBE is planned for the end of 2019 at the RT-13 at Svetloe. It will work in BRAS-compatible mode, producing four 512 MHz channels. We plan to equip all three RT-13 antennas with eight channel MDBEs in 2020. The firmware implementing the digital downconverter (DDC) mode has to be ready until the summer of 2020. From that time, the antenna at Svetloe will be able to participate in international VGOS observing.

4 Clock and Frequency Distribution System

The frequency and time distribution equipment with the phase calibration system is located in the RT-13 elevation cabin. The frequency distribution system transmits the 100 MHz reference frequency signal from the H-maser to consumers via a fiber-optic communication line. The equipment measures the electrical lengths of the reference frequency path from the H-maser simultaneously to the BRAS (to the MDBE in the future) and the PCAL generator. The resolution of the delay meter is 1 ps.

5 Future Plans

Currently we perform regular observations with the three RT-13s four to five times per day in S/X and S/X/Ka bands. We register up to four channels with 512 MHz bandwidth and a total data rate of 8 Gbps. The average recorded data rate is 8 TB per day in 24/7 mode. In 2020 we plan to participate in international VGOS observing by using the RT-13 at Svetloe.

References

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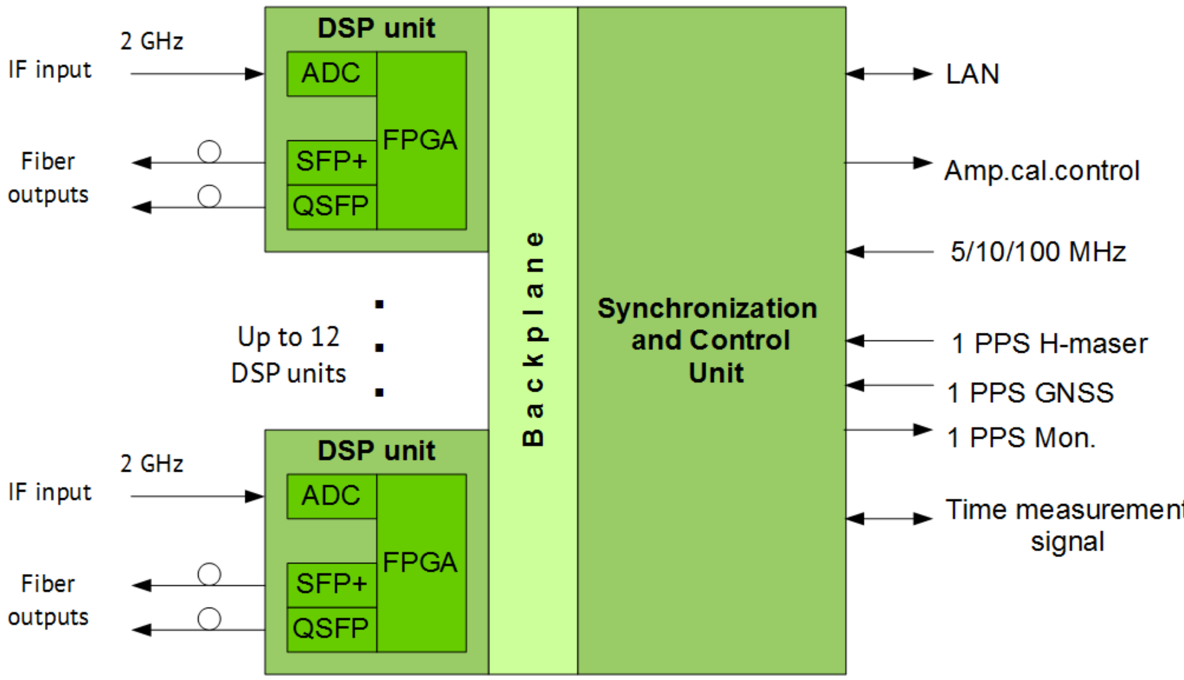

Fig. 1 MDBE structure.

Fig. 2 DSP unit without radiator, front-end board, and front panel.

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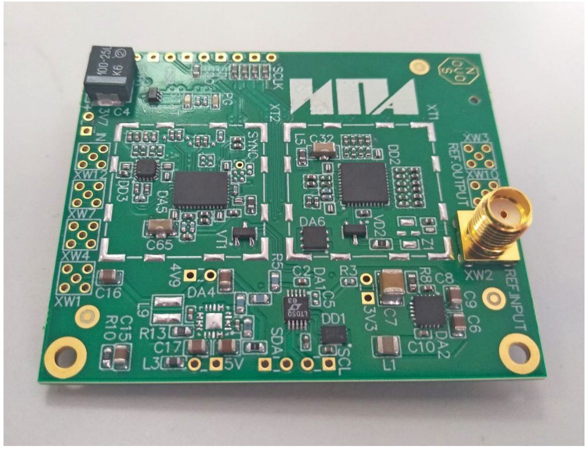

Fig. 3 Clock synthesizer without shields.