RDBE Setup and Operations

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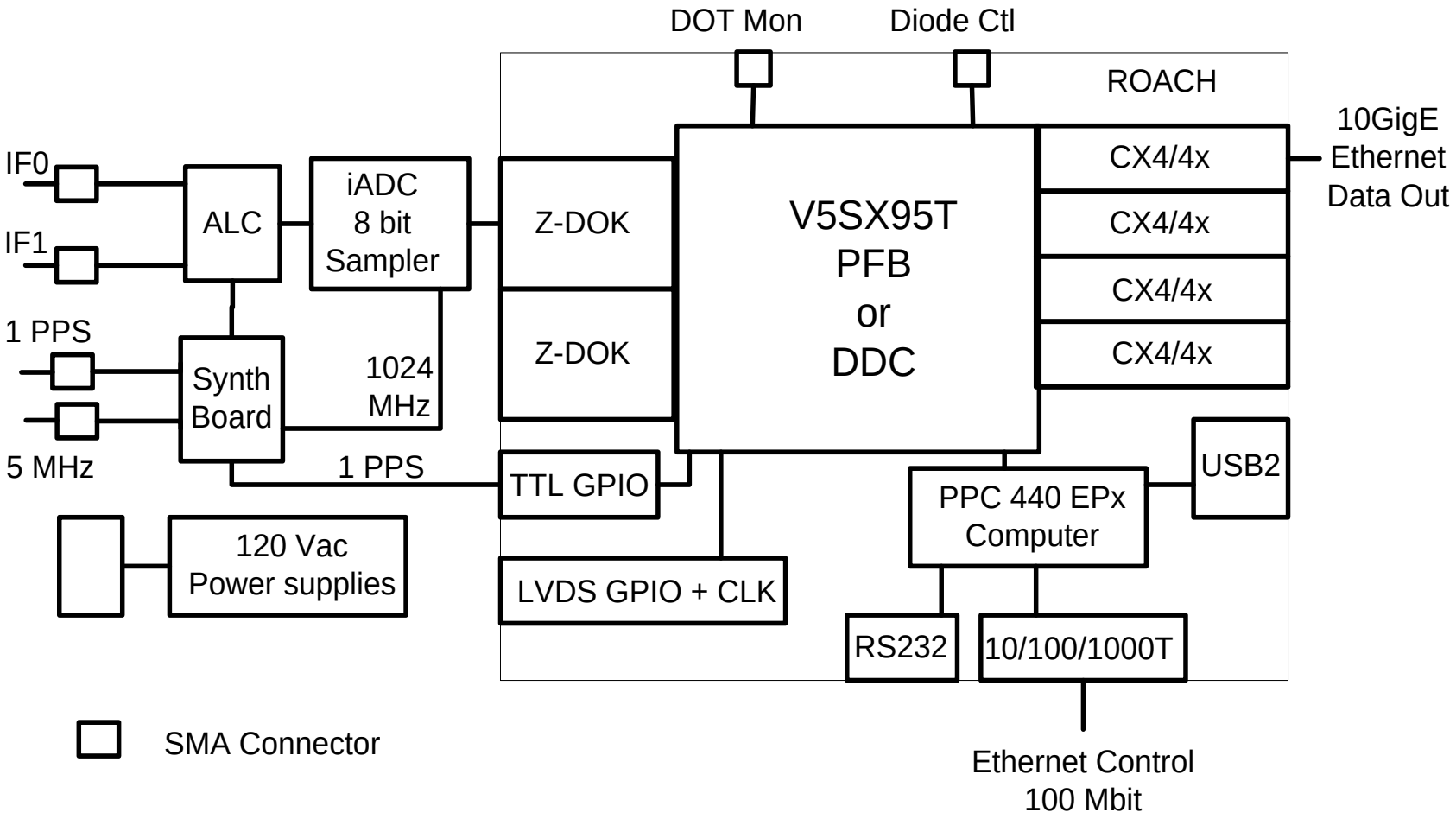
Agenda

- System overview
  - Hardware components
  - Firmware components
  - Software components
- Features
- Command set
- Basic operation
- Demonstration

System Overview

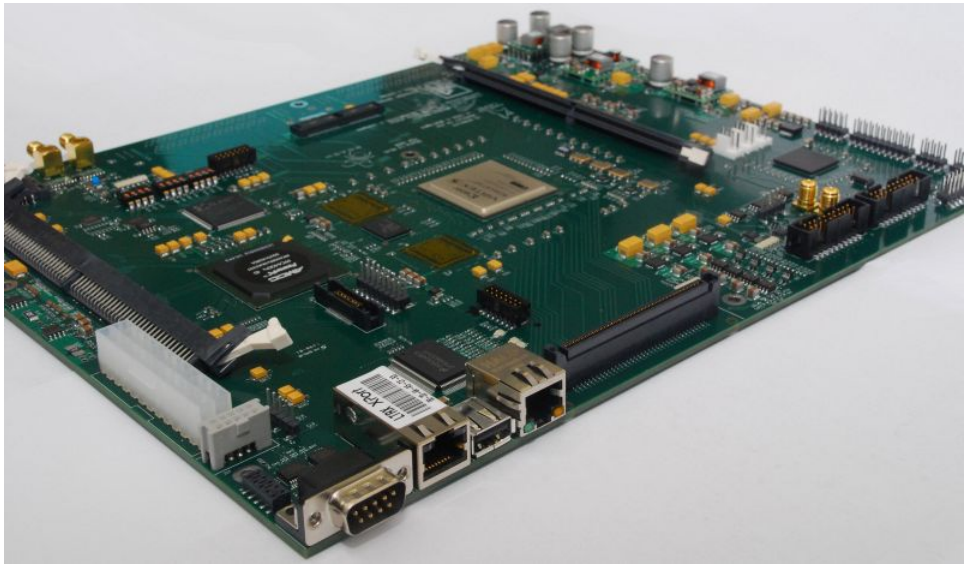
- RDBE – ROACH Digital Backend System
  - Joint collaboration between NRAO and Haystack
  - Name is assigned to a specific base system
    - Specific hardware components
    - Can be ordered from Digicom
  - Variations are expected
    - Represented by hyphenating the name **RDBE-X**
      - **X** represents the hardware components of the RDBE
    - Presently there are RDBE-H, RDBE-S
    - This overview covers the RDBE-H

RDBE-H Block Diagram



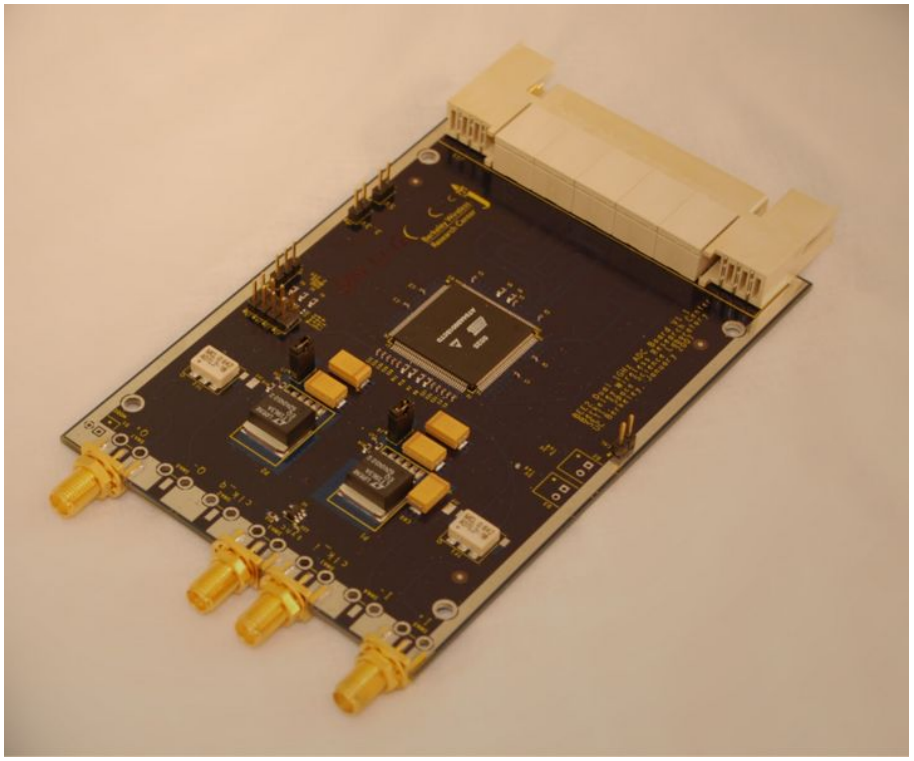
RDBE Hardware Components

- ROACH Board
  - **R**econfigurable **O**pen **A**rchitecture **C**omputing **H**ardware
  - Developed by the CASPER group at Berkeley / NRAO / KAT
- Virtex 5 FPGA
- 440 PPC processor
- 2G RAM
- 2 ZDOK connectors
  - iADC
- RS232 interface
- 1G / 100M Ethernet
- 4 CX4 10G Ethernet ports
- 1 XPORT interface



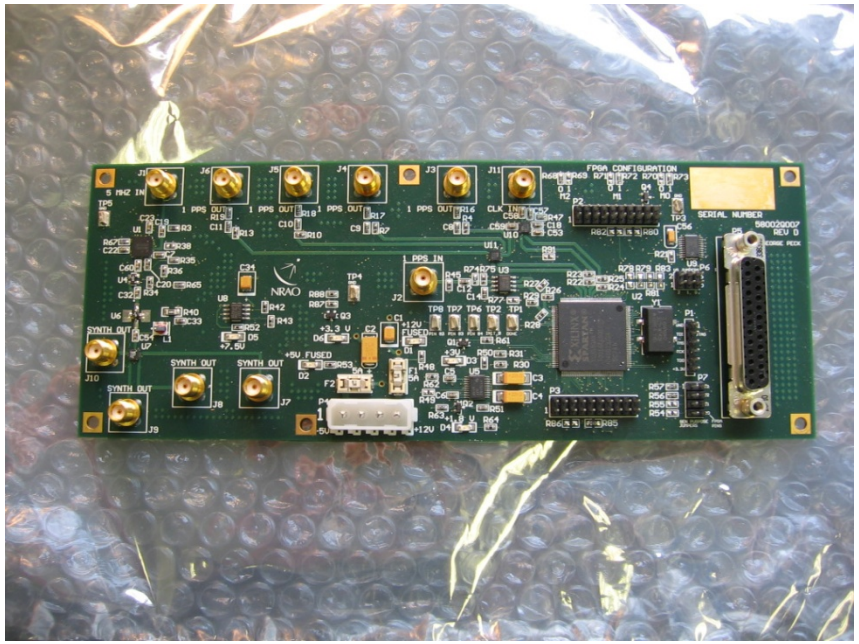
RDBE Hardware Components

- iADC
  - Analog to Digital Converter (sampler board)
    - Developed by the CASPER group
  - 2GHz bandwidth
  - 1 Gigs sample / sec
  - 8 bits / sample
- 2 iADC cards supported per ROACH



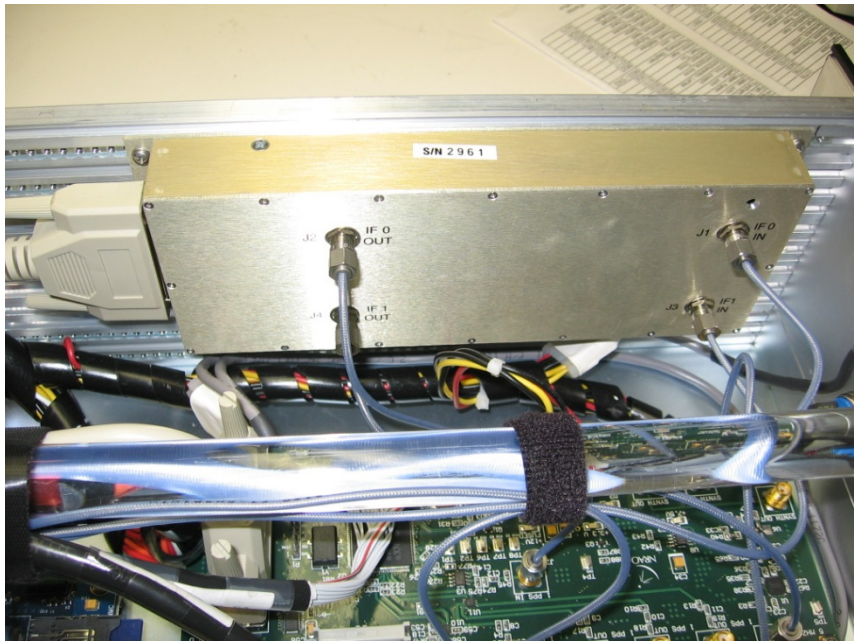
RDBE Hardware Components

- Synthesizer / timing board
  - Developed NRAO
  - Inputs
    - 5MHz
    - 1pps
  - Outputs
    - 1pps
    - 1024 MHz
  - Provides serial communication interface to ALC board



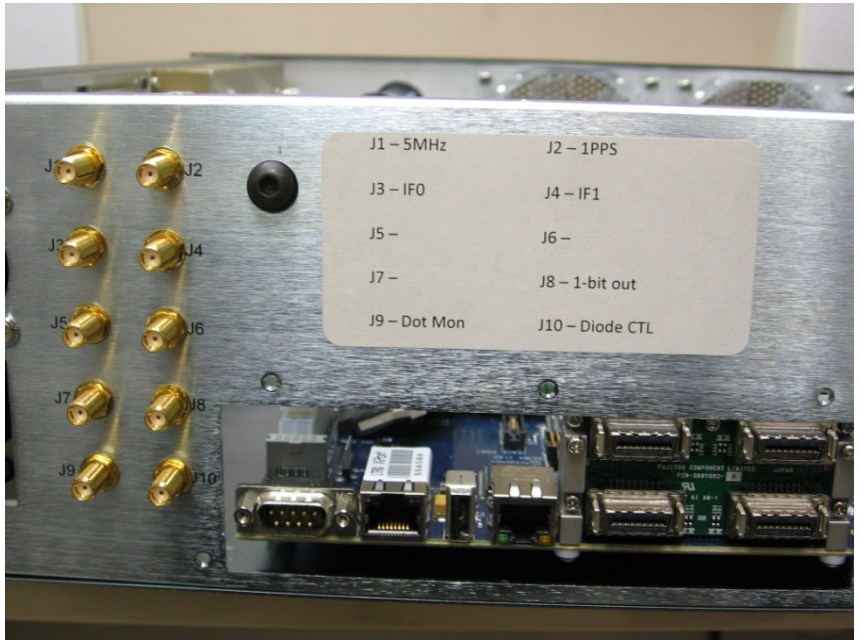
RDBE Hardware Components

- ALC
  - Analog level control
  - Developed by NRAO
  - 2 IFs in / 2IFs out
  - 0-31 dB attenuator
  - Additional 20dB solar attenuator



RDBE Hardware Components

- Miscellaneous
  - Power supply
    - 90 ~ 132 VAC or 180 ~ 264 VAC auto sensing
  - 1pps LED
    - Indicates 1pps to synthesizer board
  - Power LED
  - 10 SMA connectors



RDBE-H Back Panel

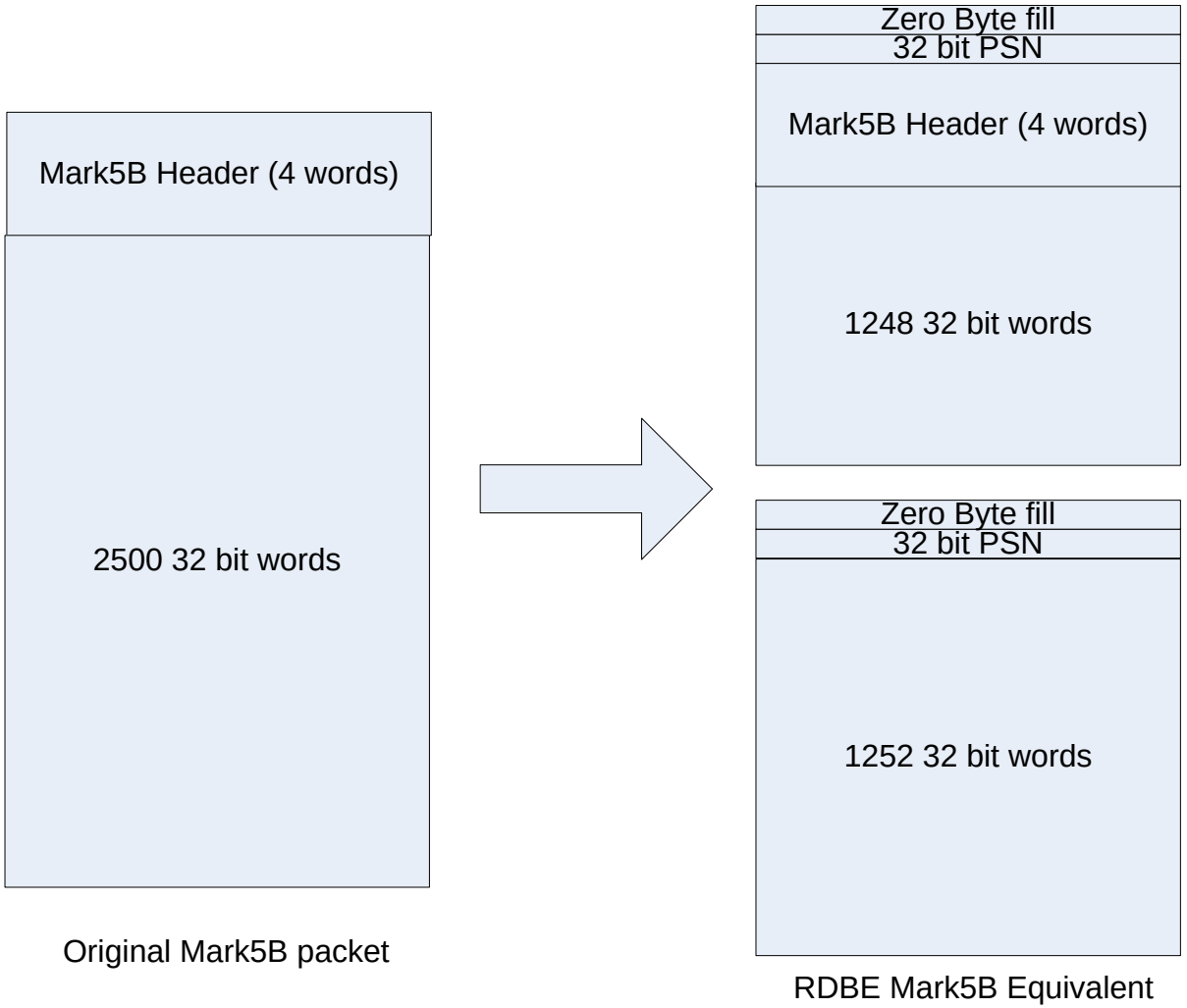
RDBE Firmware

- 3 Personality types (FPGA code)
  - Polyphase filter bank-geodesy (PFBG) Version 1.4
    - Input is two 512MHz IFs
    - Output is sixteen of 32 possible 32-MHz channels
    - Output is a 5008 byte Mark5B data format (next slide)
  - Polyphase filter bank-astronomy (PFBA)
    - Input is four 512 MHz IFs
    - Output uses two of the four 10Gbps CX4 interfaces
      - 2-bit quantized
      - 4Gbps / interface
      - 8224 byte packets using the VDIF format.

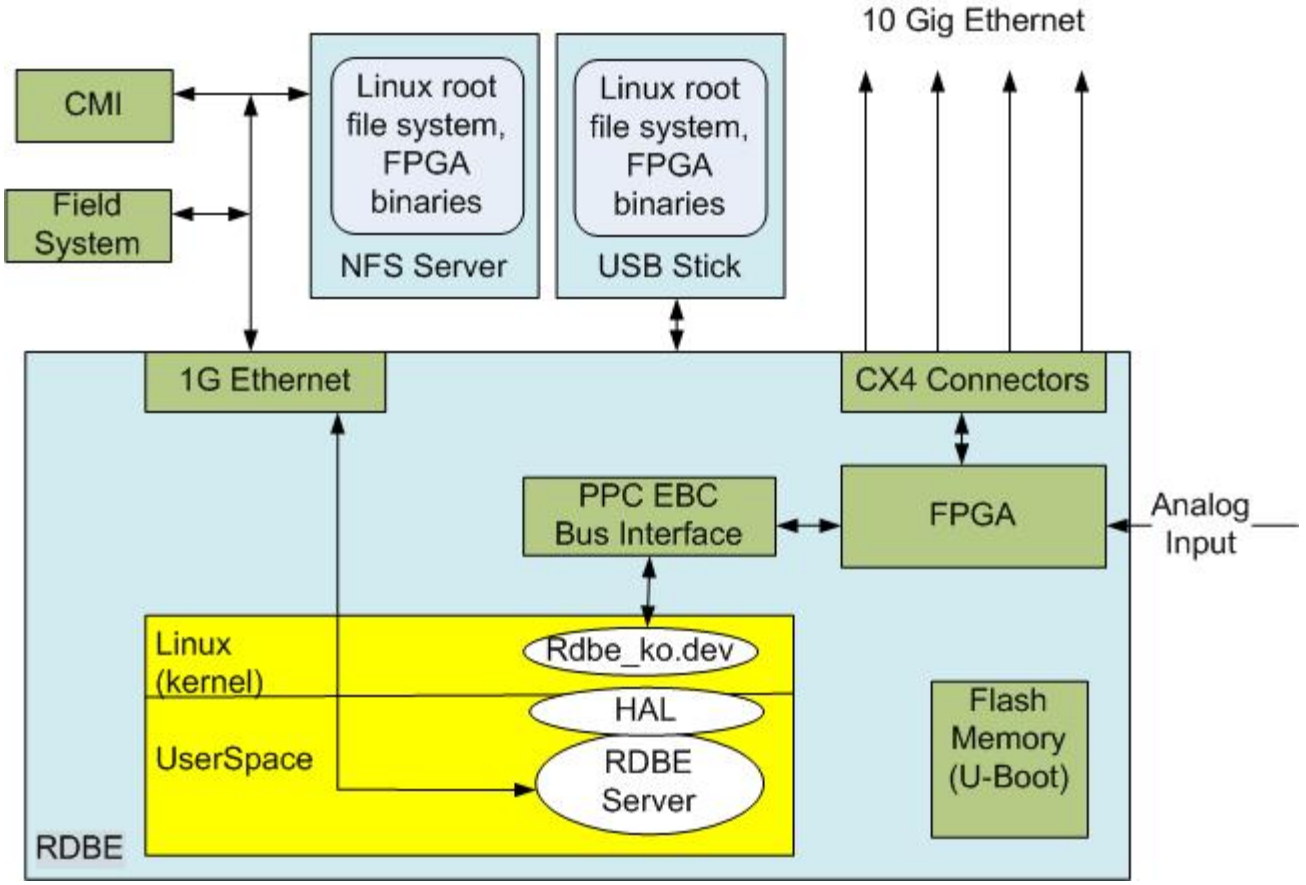
RDBE Firmware

- Digital down converter (DDC)
  - Input is two 512MHz IFs
  - Output is four tunable channels
  - Bandwidths 128 / 64 / ◦◦◦ / 1 MHz (same for all 4 channels)
    - Data rate proportional to bandwidth
  - Tunable in 15.625 kHz quanta (testing incomplete)
  - Output is in 5008 byte Mark5B format 2 bits / sample
  - 250-kHz common quantum with 10-kHz on legacy systems

Mark5B Payload



RDBE Software



RDBE Software

- rdbe_dev.ko
  - Linux kernel device driver
  - Allows the application to read / write to the FPGA personality
- HAL
  - Hardware abstraction layer
  - Allows the personality to change without changing the application software
- rdbe_server
  - Version 1.15 will be required for operation with FS
  - Accepts VSI-S commands
  - Verifies and takes actions on valid commands
  - Specified in the RDBE command set

RDBE Command Set

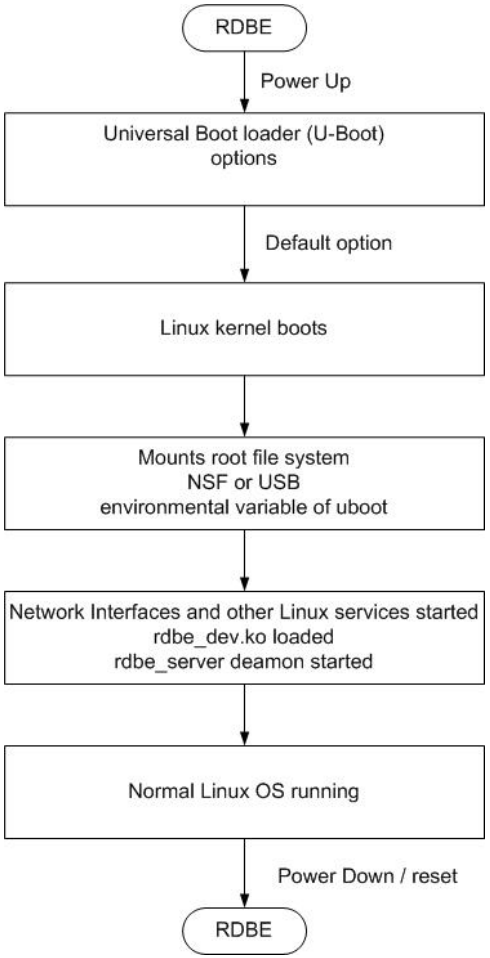
- Standard VSI-S command format
- http://www.haystack.edu/tech/vlbi/mark5/mark5_memos/091.pdf

dbe_1pps_mon	Set the 1pps monitoring broadcast state
dbe_alc	Set / get the ALC attenuator setting for INPUT 0/1
dbe_alc_pps?	Station 1pps status (query only)
dbe_alc_fpgavers	Get the ALC boards FPGA bit code version (query only)
dbe_arp	Set / get the IP to MAC address resolution
dbe_data_connect	Set / get the destination IP the data is being sent
dbe_data_format	Set the packet format mode to either the VDIF native mode or Mark5B compatibility mode
dbe_data_send	Transmit a data stream out of the DBE 10G interface
dbe_dc_cfg	Setup down-converters
dbe_dot?	Get the Data Observable Time (DOT) clock information (query only)
dbe_dot_inc	Increment the DOT clock
dbe_dot_set	Set the DOT clock on next 1pps tic
dbe_execute	Execute specific command on the DBE
dbe_hw_version?	Get the hardware version information from the DBE
dbe_ifconfig	Set / get DBE 10G network interface configuration
dbe_ioch_assign	Set / get the input to output channel assignments
dbe_packet	Set / get packet transmission criteria
dbe_personality	Set / get the RDBE FPGA bit code personality
dbe_quantize	Set / get present channel quantization data
dbe_status?	Get system status (query only)
dbe_sw_version?	Get the software version information from the DBE
dbe_tsys_mon	Set the Tsys monitoring broadcast state
dbe_xbar	Set/get the DDC crossbar switch positions

Basic Operations

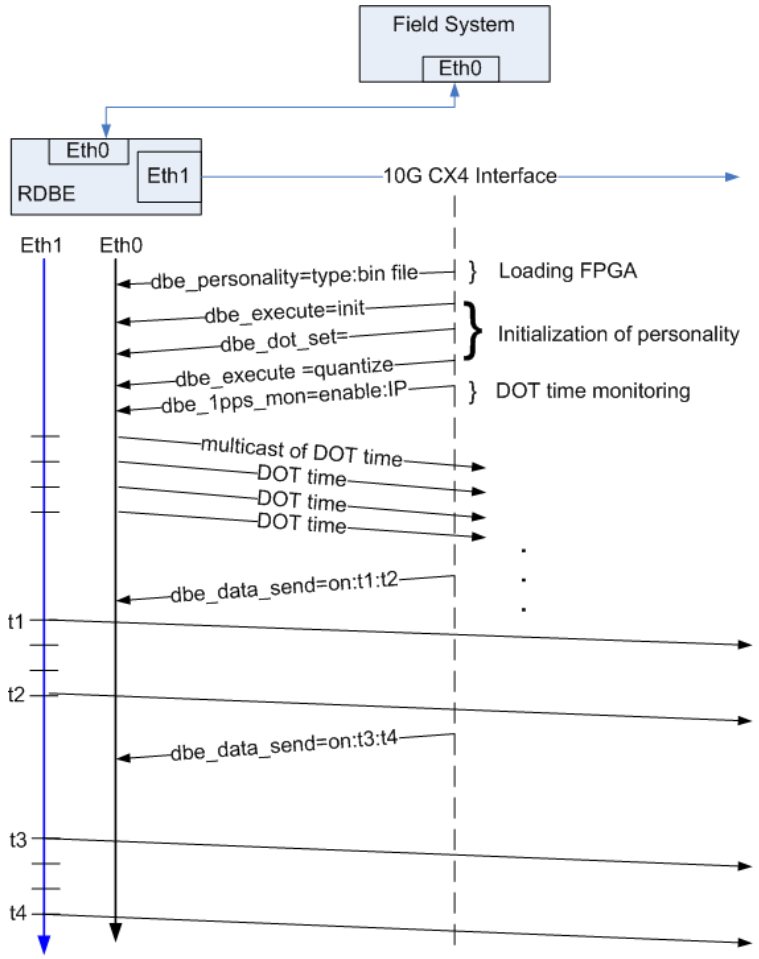
- Topics addressed on the following slides
  - Boot Up
  - rdbe_server daemon communication
    - dbe_data_send operational modes
    - raw capture mode
    - monitoring capabilities
      - 1pps
      - tsys
  - Software utilities

Boot Up



- U-Boot options
  - Environment variables defining what the boot loader will execute
    - location of the kernel in flash (address)
    - location of the root file system
      - USB
      - NFS
      - SDRAM
      - bootp
    - Network configuration
      - Static
      - Dynamic
  - Details are beyond the scope of this talk
    - Detail documentation available if needed

rdbe_server



- Loading the FPGA personality
  - Located where the root file system is mounted
  - /home/roach/personalities
- Initialization
  - Setting the FPGA registers
  - Setting the DOT time
    - system time
    - manually
  - Quantization
    - Formats the filter bank channels at 2 bits / sample
  - Monitoring capabilities
- Set for normal operations
  - Transmitting data out CX4 interface
  - Status / etc.

IO Channel Assignment

- Capability to set the input output channel assignment for the VLBI Payload
  - Feature for PFBG personality only
    - Input is two 512MHz IFs
    - Output is sixteen of 32 possible 32-MHz channels
  - The command
    - dbe_ioch_assign = <input>:<channel(s)>: [<threadID>] : … [<input>]:[<channel(s)>]: [<threadID>] ;
    - input
      - 0 or 1 for IF0 or IF1
    - channel(s)
      - Either individual channels or a range of channels
    - threadID
      - vdif specific and presently ignored

IO Channel Assignment

- The channel ordering
  - Directly related to the assignment combination
    - input and channel specified in this command
  - The present geodetic personality
    - dbe_ioch_assign? returns
      - dbe_ioch_assign ? 0: 0:1: : 1:1: :0:3::1:3:…0:15: :1:15: ;
      - with the first input / channel combination 0:1
      - assigned to the least significant position in the data array format (bit 0,1)
      - the most significant bits being assigned to input 1 channel 15

IO Channel Assignment

- A common setting used for testing with DBBC
  - dbe_ioch_assign = 0: 0-15 ;
  - Assigns all of IF0s 32 MHz channels to the VLBI Payload
  - dbe_ioch_assign? returns
    - dbe_ioch_assign ? 0: 0:1: : 0:2: :0:3::0:4:…0:14: :0:15: ;
      - with the first input / channel combination 0:1
      - assigned to the least significant position in the data array format (bit 0,1)
      - the most significant bits being assigned to input 0 channel 15

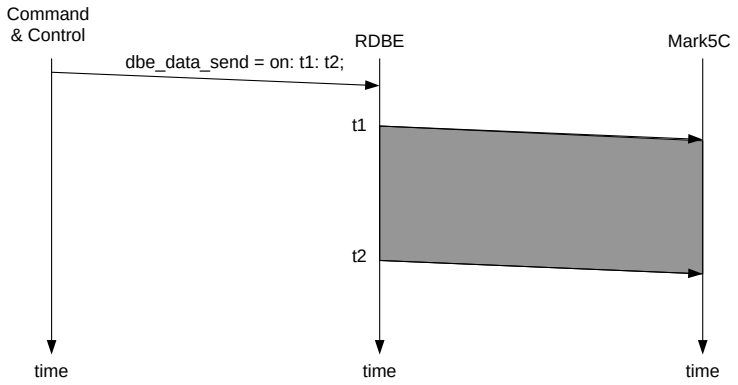
Data Transmission

- In the past data were always available and the gating function was performed on the recording device
  - Record = on / off commands
- A new approach has been taken for when to transmit data out of the interface
  - Since the start and end time are known apriori
    - use the dbe_data_send to gate the output on the 10G
    - past option is still available

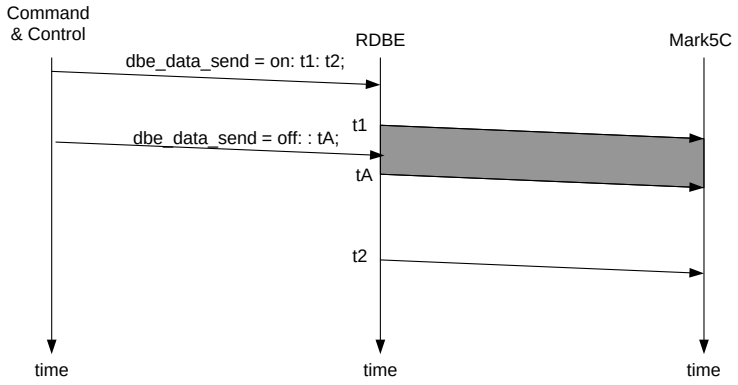
Design Philosophy

- start time <= present DOT time < end time
  - Personality will transmit valid packets
  - Times are specified as integer seconds
- Start and end times are programmed into the FPGA using the command:
  - dbe_data_send
  - command format
    - dbe_data_send = < state > : [< ts >] : [<te>] : [<delta>];
      - state - either “on” or “off”
      - start and end times (ts, te) are of the format YYYYDDDHHMMSS
      - delta - specified in integer seconds.

dbe_data_send options



- Specify start / end time
  - YYYYDDDHHMMSS
- Or specify start and delta time
  - t2 is generated as t1 + delta
  - delta is integer seconds

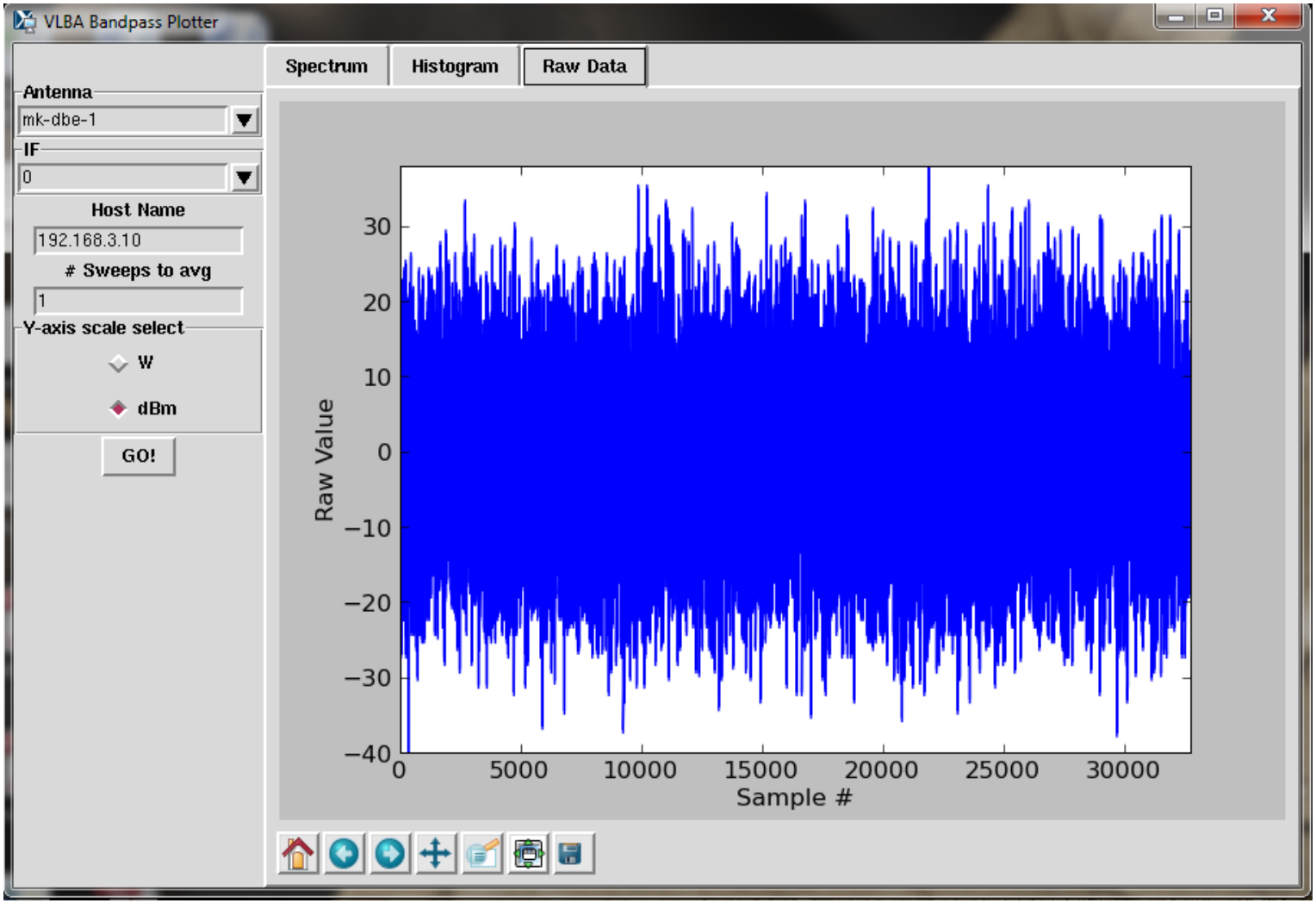


- Ability to abort an active transmission
  - send the off state with
    - a specified time
    - no time - meaning next integer second

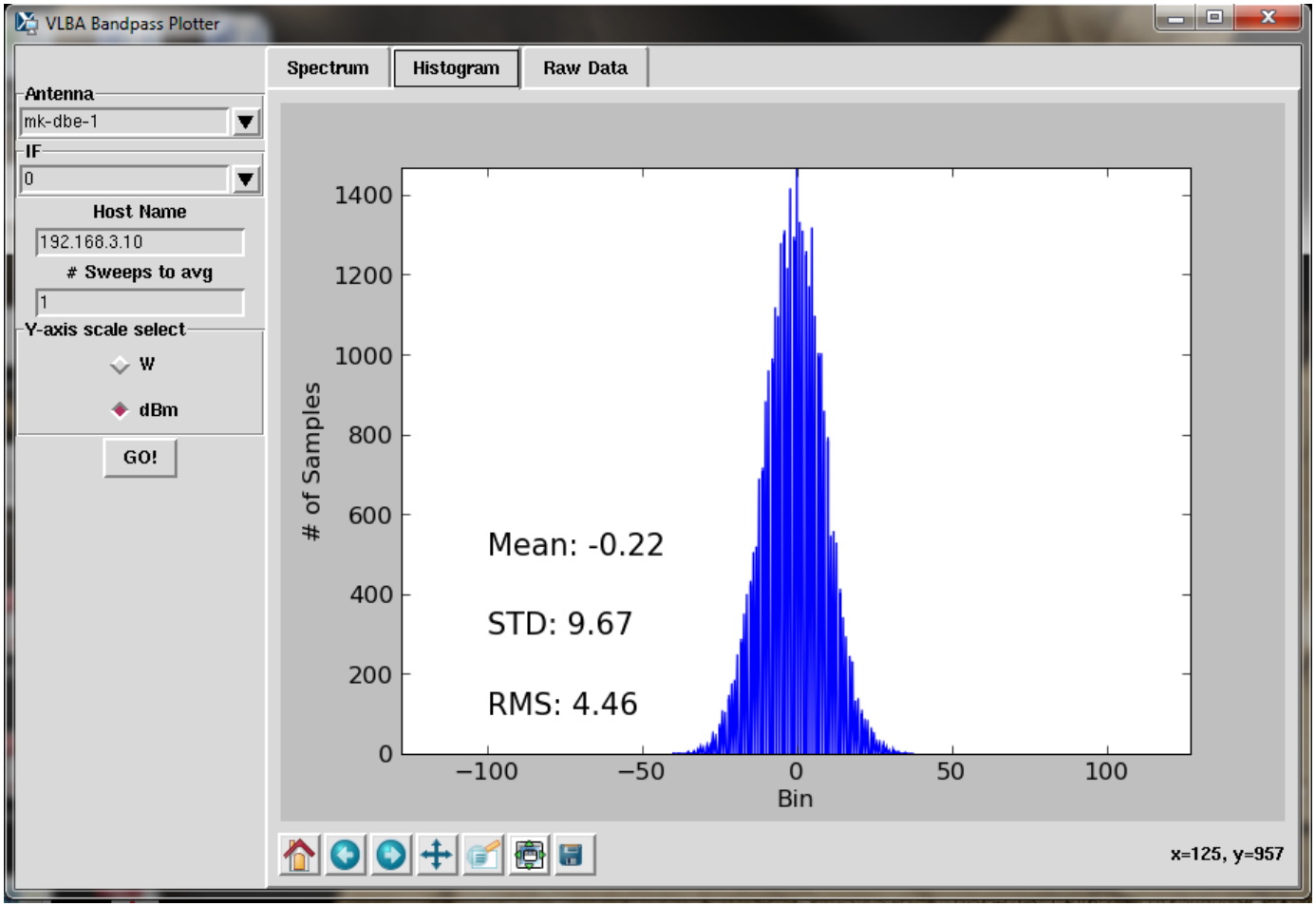
Raw Capture Mode

- Provides ability to see the incoming signal from the iADC before it is processed by the FPGA personality
- It is a separate thread within the rdbe_server
  - Listening on port 5000
  - Responds to a client requesting a specific IF to capture
    - 32000 samples are captured
    - the raw data are returned to the calling client to be processed
      - by software utility “bpplotter”
        - » developed by NRAO

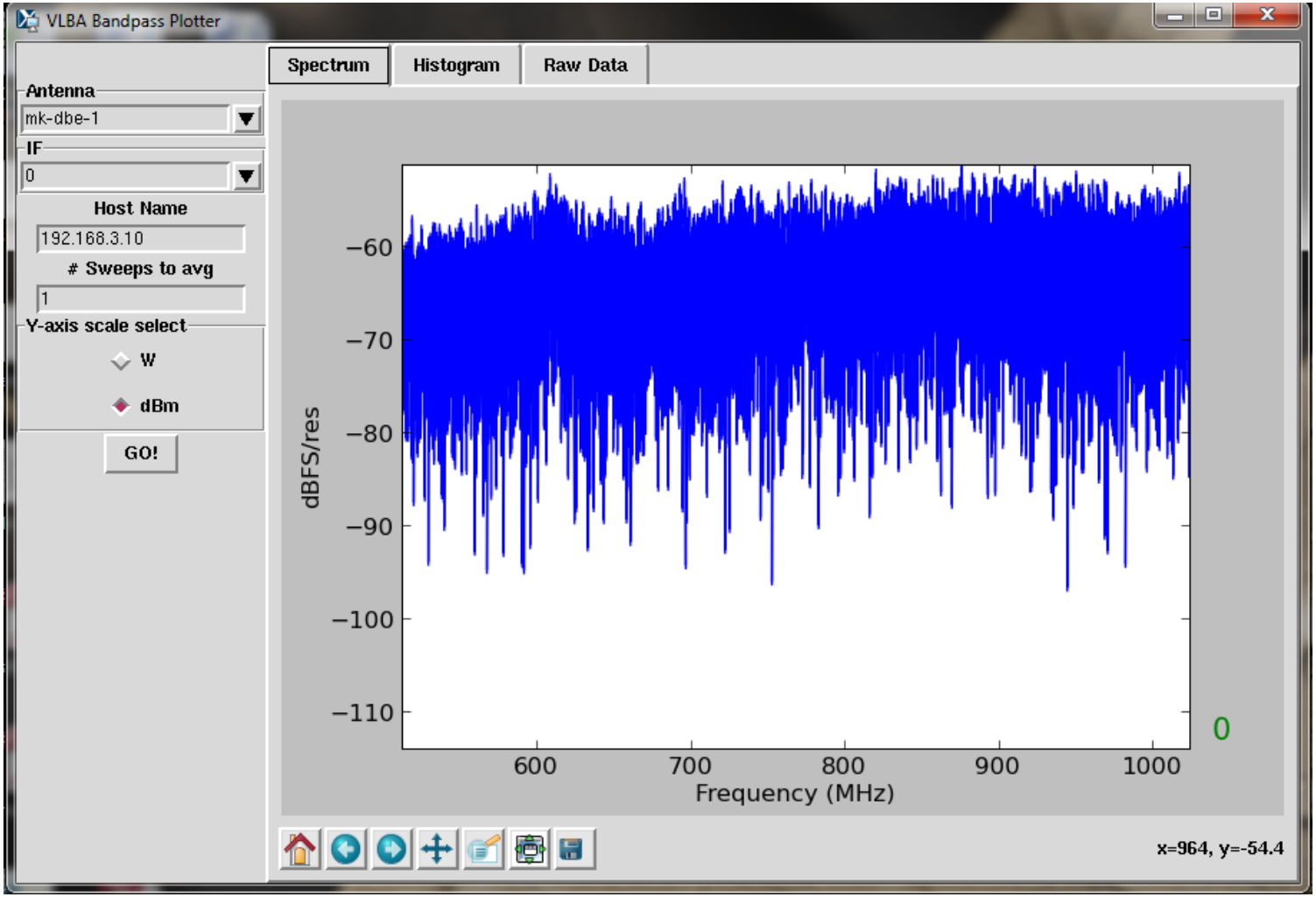
bpplotter


VLBA Bandpass Plotter
Spectrum
Histogram
Raw Data
Antenna
mk-dbe-1
IF
0
Host Name
192.168.3.10
Sweeps to avg
1
Y-axis scale select
W
dBm
GO!
Raw Value
30
20
10
0
−10
−20
−30
−40
0
5000
10000
15000
20000
25000
30000
Sample #

bpplotter


VLBA Bandpass Plotter
Spectrum
Histogram
Raw Data
Antenna
mk-dbe-1
IF
0
Host Name
192.168.3.10
Sweeps to avg
1
Y-axis scale select
W
dBm
GO!
# of Samples
Bin
Mean: -0.22
STD: 9.67
RMS: 4.46
x=125, y=957

bpplotter


VLBA Bandpass Plotter
Spectrum
Histogram
Raw Data
Antenna
mk-dbe-1
IF
0
Host Name
192.168.3.10
Sweeps to avg
1
Y-axis scale select
W
dBm
GO!
dBFS/res
−60
−70
−80
−90
−100
−110
600
700
800
900
1000
Frequency (MHz)
0
x=964, y=-54.4

Monitoring Capabilities

- 1pps monitoring
  - dbe_1pps_mon = <enable> : <multicast IP address> : <port>;
  - Use gDot.py on a system attached to same network to receive multicast data
- Tsys monitoring (version 1.4 of fpga code)
  - System temperature measurement
  - On power / off power of the receive chain
  - dbe_tsys_mon = <enable> : <multicast IP address> : [<port>] : [<interval>];
    - default interval is 6 secs
    - tsys data is summed every second
  - dbe_tsys_diode_ctl must be set to use above function
  - Use tsys.py for gathering data

Software Uilities

- *rbde_client -h <machine>*
  - Command line interface to RDBE
  - *-h <machine>* is the target RDBE systems IP address (defaults to localhost).
  - *rdbe_server* must be running on *<machine>*
- *rdbe_gui*
  - *G*raphical client interface to the RDBE

Software Uilities

- *gDot -h <multicast address>*
  - A graphical multicast 1pps time receiver
    - that displays the broadcast DOT time
  - The RDBE server must be configured
    - with the dbe_1pps_mon command.
- *power_est_client -h <machine>*
  - *A* command line client
    - calculates the mean, standard deviation and maximum power of a specified input IF into the RDBE.
    - the input IF is selected by sending a 0 or 1 at the command prompt.

DEMONSTRATION

TIME PERMITTING