

RDBE Development and Progress

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Abstract

A digital backend based on the ROACH board has been developed jointly by the National Radio Astronomy Observatory and MIT Haystack Observatory. The RDBE will have both Polyphase Filterbank and Digital Downconverter personalities. The initial configuration outputs sixteen 32-MHz channels, comprised of half the channels from the PFB processing of the two IF inputs, for use in the VLBI2010 geodetic system and in the VLBA sensitivity upgrade project. The output rate is 2×10^9 bits/second (1×10^9 bits/sec = 1 Gbps) over a 10 GigE connection to the Mark 5C with the data written in Mark 5B format on disk.

1. The RDBE Development

The need for increased accuracy and sensitivity in radio astronomy has led to the development of primarily digital systems for the complete backend. The first digital backend developed at Haystack Observatory, called the DBE1, was based on the CASPER iBOB. Data were output at a rate of 2 Gbps on VSI-H connections from each of two IF inputs, writing each to a Mark 5B+ for a total data rate of up to 4 Gbps. The digital signal processing utilized a polyphase filterbank (PFB) approach to provide sixteen channels of 32 MHz bandwidth from each IF. However, the size of the FPGA on the iBOB inhibited the addition of any other capabilities. At the same time, NRAO was seeking an optimal approach to a digital backend for its VLBA Sensitivity Upgrade project. Thus, a collaborative development was initiated, with the hardware design and construction led by NRAO and the software/firmware development led by Haystack. NRAO collaborated separately with the South African KAT project and the UC Berkeley CASPER Laboratory to develop the ROACH hardware platform for the new RDBE (ROACH Digital BackEnd).

Some of the achieved and planned features of the RDBE are:

- PFB channelization into sixteen 32-MHz channels from each 512 MHz IF:
 - each IF output to one Mark 5C (4 Gbps total output rate) (in development)
 - eight channels from each IF combined on one output (2 Gbps total rate) (complete)
 - selection of which eight channels are recorded from both IFs (the same eight) (complete)
- output over one or two 10 GigE Ethernet ports:
 - Mark 5B format (complete)

- VDIF format (in development)
- threshold adjustment to obtain proper state statistics for each 32 MHz channel (complete)
- adjustable input attenuator setting for level control to the samplers (complete)
- synchronous detection of the added power from a noise diode for system temperature measurement (in development)
- implementation of a digital down-converter personality (in development)
- phase cal signal extraction (planned)

2. The RDBE Structure

The basic components of the RDBE are the input Analog Level Control (ALC) board, samplers (iADC), ROACH board, and a synthesizer/timing board. The iADC was developed by the CASPER Laboratory, while the ALC and synthesizer board were developed by the NRAO-Socorro Electronics division. A schematic of the physical organization of the RDBE is indicated in Figure 1. The fully constructed RDBE is shown in Figure 2a.

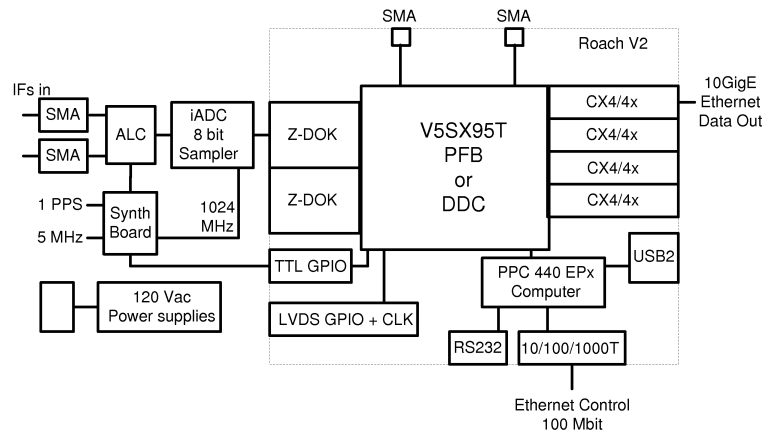


Figure 1. Layout of the RDBE.

A functional block diagram is shown in Figure 2b. The inputs are one or two 512 MHz data lines, a 1-pulse-per-second signal, and the 5 MHz reference frequency from which the 1024 MHz clock rate is synthesized. The digital signal processing of the RDBE is carried out in a XILINX SX95T-1 FPGA chip on the ROACH board, which is programmed in VHDL. Commands (which must follow VSI-S standards) and communications are received and transmitted over a 1 Gbps Ethernet to the Power PC on the ROACH board. The commands, defined in the DBE command set document (in preparation), are processed by the RDBE Application Server and passed to the FPGA via the Hardware Application Layer (HAL) over the external bus control (EBC) interface. This method was adopted to isolate the FPGA firmware from the PPC software applications, thus allowing different FPGA personalities (e.g., PFB or DDC) to be loaded without modifying the software. Having been processed by the PFB or DDC firmware in the FPGA, the data are output through one or two 10 GigE ports on CX4 connectors.

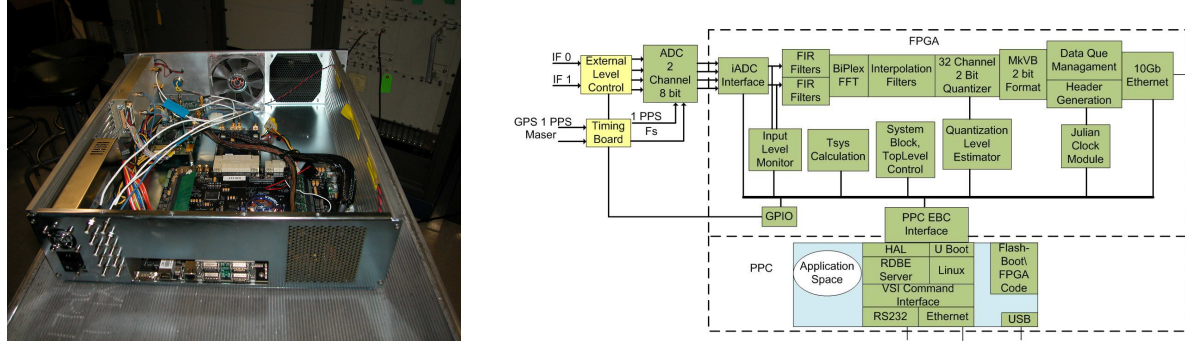


Figure 2. a) The RDBE. b) Functional diagram of the RDBE.

3. Test of PFB Functionality in Geodetic/VLBA Mode

The PFB capability of the RDBE has been demonstrated in several short-baseline VLBI tests, without many of the functions required for an operational system. For these tests, the signal from each IF was filtered to be in the second Nyquist zone of the iADC (512-1024 MHz) and thus appears as net lower sideband. The PFB FPGA personality (functionality) selected eight odd-numbered channels (1, 3, ..., 15) from both IFs and interspersed them in the output stream, thus producing sixteen 32-MHz channels. Output to the Mark 5C recorder was transmitted through one 10 GigE port at 2 Gbps in Mark 5B format. Data were recorded in parallel using existing systems to verify that the setups were correct in case the RDBE/Mark 5C failed to produce fringes.

Tests by Haystack used RDBEs at the 18-m Westford, MA, antenna and at the 5-m MV3 antenna in Greenbelt, MD. These two antennas are separated by approximately 800 km and have been used extensively for testing the VLBI2010 broadband proof-of-concept system ([1]). Both antennas used the broadband system, with a DBE1 and Mark 5B+ as output for one band, and an RDBE and Mark 5C processing and recording signals from the other. The data were correlated on the Mark IV correlator at Haystack. A single scan on the source 4C39.25 was used to validate the basic functionality of the RDBEs. The observations were made in the frequency band 8.6 to 9.1 GHz, and fringes were found within one microsecond of the expected clock difference as measured relative to GPS at each site

Tests by NRAO used RDBEs and Mark 5C units, installed in parallel with the existing equipment, in a “piggyback” mode during normal VLBA observations. Fringes from a continuum calibrator, 0823-223, were detected in the 8.6-9.1 GHz band between the Los Alamos and Pie Town stations, using the VLBA’s DiFX correlator. Single-dish spectra of 22-GHz water masers in Orion A were also obtained at Los Alamos.

4. Next Steps

Several important functions remain to be implemented before the PFB personality can be used operationally.

- Access to the 1 second marker within the FPGA for processing by the PPC. This will enable display of the actual time being encoded in the data output stream at the beginning of each second, as well as comparison with GPS time.

- Measurement of system noise temperature in each channel by synchronously detecting the power from a noise source, injected in the front end at a switch rate of 10 to 100 Hz.
- Support for other 2-Gbps channel subsets, in addition to the alternating channel scheme used in the tests.

In addition to the PFB personality implemented at Haystack, a digital down converter (DDC) personality is being developed at NRAO. It is expected that up to sixteen DDCs will be supported, with bandwidths between 0.0625 MHz and 128 MHz (with the number of DDCs times the bandwidth not exceeding 512 MHz). The DDCs will be tunable to any frequencies covered by the two IFs, and each DDC can be either upper or lower sideband.

Longer-term PFB data processing capability is also being planned.

- Extraction of phase cal tones
- Output in VDIF format [2]
- Output of each IF through a CX4 to a Mark 5C (4 Gbps total on two Mark 5Cs)
- Output of both IFs through one CX4 to one Mark 5C (4 Gbps total); this requires completion of so-called non-bank mode recording in the Mark 5C (spreading the input data across two modules).
- The addition of a second iADC to the ROACH board to accept a total of four 512 MHz IFs; production of a single 512 MHz channel from each for a total data rate of 8 Gbps out of two CX4s.

5. Acknowledgments

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