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DBBC VLBI2010

Gino Tuccari [1], *Walter Alef* [2], *Alessandra Bertarini* [3], *Salvatore Buttaccio* [1], *Giovanni Comoretto* [4], *Dave Graham* [2], *Alexander Neidhardt* [5], *Pier Raffaele Platania* [1], *Antonietta Russo* [4], *Alan Roy* [2], *Michael Wunderlich* [2], *Reinhard Zeitlhöfler* [6], *Ying Xiang* [7]

[1)] *Istituto di Radioastronomia – INAF*
[2)] *Max-Planck-Institut für Radioastronomie Bonn*
[3)] *Institut für Geodäsie und Geoinformation, Universität Bonn*
[4)] *Osservatorio di Arcetri – INAF*
[5)] *FESG München*
[6)] *BKG Wettzell*
[7)] *Shanghai Astronomical Observatory – CAS*
Contact author: Gino Tuccari, e-mail: g.tuccari@ira.inaf.it

Abstract

The DBBC2 backend system has been adapted for supporting the VLBI2010 demands. The system architecture for this application is presented.

1. Introduction

The VLBI2010 geodetic world is rapidly evolving, and a better delay estimation will be obtained using a collection of strategies including a much different antenna-receiver-backend system. Wider portions of band will be used, extracted from a very wide sky frequency range.

A pretty different backend is required, which is able to handle a higher data rate and has enough capability to down-convert a larger number of wide bandwidth channels in appropriate mode for correlation.

The DBBC system is modular in hardware and firmware, allowing it to realize an architecture able to include everything necessary to support the new VLBI2010 observational needs. The system in this implementation was named DBBC2010.

2. Architecture

A number of eight bands coming from the receiver represent the information input to the DBBC2010 backend. These are portions of band, 500 or 1000 MHz wide, down-converted with analog methods from a receiver able to observe between 2 and 15 GHz. So the first important difference with respect to a standard DBBC2 is the number of IFs the system needs to support: an increase from four to eight.

It was felt important that the total space for supporting the entire functionality would not be modified and so simple mechanical solutions have been required to handle the doubled number of input IFs.

The four Conditioning Modules have been then mechanically modified in order to handle two UNICA3 boards in the same space. Additionally a development is underway in order to reduce the filter size in the board and integrate all the amplification functionalities. As a result of all of this, eight input bands are conditioned and available internally to the system for further processing.

Twice the number of IFs requires twice the number of sampling boards. There are two possibilities, or to be more precise, three. The width of instantaneous bands can be selected between 512 MHz and 1024 MHz, but it was also introduced the possibility to handle 2048 MHz wide pieces of band, adopting the ADB3 sampling module. Such module is a stack of two ADB2 boards with an accompanying element, to make the sampling boards able to operate interleaved with a 2048 MHz clock. Nyquist input bands possible are 10–2048 MHz and 2048–3500 MHz. The output of such module is an aggregate of eight data busses to be sent in the standard HSI bus to the processing boards.

In order to have eight ADB sampling boards operating, it needs to have a doubled number of sampling clocks and related high resolution 1PPS signals, all of this operating at 1024 or 2048 MHz. This was realized with the new CAT2 board, where in a single PCB all the functionalities are present to generate clock and timing for the entire system, driven by the internal DBBC PC set.

At this point we have internally available a number of eight IFs in digital representation, ready to be introduced in the processing boards for the fixed band (FT) down-conversion. The difference is that we have twice the number of bands to handle now. Again we have more options to consider. A number of Core2 boards could be adopted to process the block of eight IFS, but if we need a much more efficient and cheaper method, the Core3 could be considered for this massive data handling.

The Core3 board is an evolution of the present Core2 processing board. It is mainly devoted to very high demanding processing capabilities. It is planned to be used as digital preprocessor for L2C polarization conversion and in applications like a very-high-number-of-channels spectrometer. For the VLBI2010 FT configurations with 1 or 2 GHz input bandwidth it looks like a very appropriate choice. In the DBBC2010 architecture it needs to have between two and four Core3 boards for processing all the eight IFs, depending on the instantaneously selected input bandwidth, as we have seen ranging between 512 and 2048 MHz. The Core3 hardware has been fully defined, and it is expected to have the boards available and tested before the end of 2010.

After the digital down-conversion we have a pretty high number of channels to handle. Let's have a look at how they aggregate. The clock accompanying the data is 64 MHz, and each 512 MHz is divided into 15 channels 32 MHz wide. This means we still have several possible conditions depending on the input bandwidth of our eight IFs. If we consider 8 x 512 MHz, there are 8 times 15 channels, while if we consider 8 x 1024 MHz, there are 8 times 31 channels to be transferred to an appropriate number of recorders. The Core3 board has a dedicated output channel able to feed the FILA10G network board directly, without having to transit from any VSI connection. This means that a number of FILA10G boards can be selected considering that a single FILA10G can support two Mark 5C recorders.

3. Conclusions

What was described here is the adaptation of a standard DBBC system to the VLBI2010 needs, with the implementation architecture named DBBC2010. It is evident that the modular structure

can easily accommodate such an observational mode, while it grows in data rate capacity. The number of IFs is well selected from the start, the input bandwidth with consequent increase of data rate demand can be selected and in case of need increased, so as the number of connections to Mark 5C units considering the total data rate to be obtained. Burst mode operation is possible even with the use of piggy-back memory modules, available in both Core2 and Core3 boards.

Figure 1. FILA10G board in the DBBC system.

Figure 2. GLAPPER (glass to copper) prototype board to connect a DBBC with a Mark 5C.