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DBBC2 Backend: Status and Development Plan

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Abstract

The DBBC2 system is in a mature phase now, and the deployment is continuing. A review of the backend is shown, and the new functionalities in development are reported.

1. Hardware

The DBBC2 hardware system is composed of a class of boards able to support different platforms and thus different system configurations. In the VLBI backend implementation, mainly two observing types are required: tunable configuration and fixed contiguous bands. The first is adopted to emulate the present Mark IV terminal and is required for both geodetic and astronomical observing modes. The second is for astronomical millimeter observations and the new coming VLBI2010 geodetic modes. Both modes are required in the same terminal to be used depending on the observation to be performed, so some efforts have been put into accomplishing these modes in a unique hardware architecture.

The interface between the receivers and the backend is included in the DBBC2. It is based on the Conditioning Module, with the possibility of selecting the Nyquist band on which to operate and the total power measurements. An automatic gain control allows the regulation of the signal levels to be transferred to the analog-to-digital conversion ADB boards. Two types of such sampling elements are available with an instantaneous band for VLBI of 512 or 1024 MHz. Additional possibilities are available up to an instantaneous 2048 MHz, described in the new hardware development section (Section 3).

The ADB1 board operates with a sampling 1024 MHz clock, for converting an input signal in the range 10—2200 MHz, while the ADB2 operates at 2048 MHz with an input signal up to 3500 MHz. The ADB2 is able to operate in ADB1 mode and, moreover, can adopt as piggy-back a FILA10G board, to transfer pure sampled data using optical fibers with a 10G Ethernet connection. The ADB2 board was widely tested and is ready to be inserted in the standard DBBC2 stack.

The processing unit Core2 board is also fully operative and represents the element adopted to generate the down-converted channels in both modes: tunable and fixed tuning. The board is compatible with ADB1 and ADB2 and supports a minimal equivalent of four Core1 functionality. The pcb has 40 equivalent layers, and all the connections for signal transfer are differential, twisted, and matched in delay and impedance between the pads of the dice and the pins of the bus connectors. A piggy-back element can be adopted for additional functionalities.

One Core2 board is able to emulate the complete functionality of four analogue BBCs, or to generate a fixed tuning version of fifteen 32-MHz-wide baseband channels, covering an input 512 MHz receiver band.

The CaT2 board (Clock and Timing) is able to generate a highly flexible number of synthesized sampling clock values (e.g., 2048 MHz, 1024 MHz), phase locked with an external 10 MHz. Low phase-noise and very small sensitivity to temperature are the main performance characteristics. The board is also producing 1PPS synchronization signals for all the ADB boards and the entire digital chain. Frequency selection is performed with the DBBC2 internal PC Set.

The FiLa10G can be used as piggy-back board of any ADB2 sampler, giving the possibility to transmit and receive in the same time a high data rate of 20 Gbps + 20 Gbps. The bidirectional functionality could be required for instance when an RFI mitigation is needed to be realized in a remote position with respect to the sampling and processing site. With the typical sampling frequency of 2048 MHz and the full 10-bit data representation, a double optical fiber set meets the full data handling requirement. Moreover, the board is equipped with two additional transceivers able to operate at 1-2-4 Gbps for slower connections.

2. Firmware

The DBBC2 VHDL firmware was completely rewritten in a platform-independent fashion. This was accomplished with a great reduction in complexity producing very compact and efficient code. Performance improvement guarantees a bit-by-bit identical output from a set of BBCs belonging to the same Core2 board, having of course the same tuning settings and input data. Still some debugging is under way to check the entire new code.

The fixed tuned (FT) configuration firmware is also available: it produces a set of 16 (15 usable) contiguous 32 MHz bands from a 512 MHz input range, in any of the Nyquist zones available from the ADB1/2 boards. This configuration is available for the VLBI2010 mode or for the millimeter VLBI network.

Firmware under development covers the following tasks: a) fully tunable 1 GHz input bandwidth, b) fully tunable 2 GHz input bandwidth, c) 1 GHz FT with 31 channels 32 MHz bandwidth, and d) 2 GHz FT with 63 channels 32 MHz bandwidth.

Additional firmware configurations are under development, including a multichannel spectrometer, the linear-to-circular (L2C) polarization digital conversion, and a polarimeter. In particular the L2C configuration was fully simulated and proved efficient. Now the adequate processing board (Core3, see in the new hardware development section) is expected for taking care of the necessary processing capability.

3. New Hardware Development

New hardware parts to be integrated in the system are under development. This covers the interfacing, input bandwidth, and processing capability.

The FILA10G board is the interface between the system and the Mark 5C recorder or the network. The main connections are two optical fibers operating each at a maximum rate of 10 Gbps. In VLBI standard this is limited by 8.192 Gbps, and for the present recording capability the limitation is 4 Gbps. The data rate is fully bidirectional and compliant with standard Ethernet networks, under UDP protocol. At present the development status sees the hardware defined and available with some prototypes, and the firmware development at a good stage: VLBI VDIF and Mark 5B modes are almost complete. Some communication experiments have been done with a Mark 5C recorder.

The 10G network FILA10G board is adopting optical fibers. In order to be connected with one or two Mark 5C recorders, which adopt the copper CX4 standard, it needs to be interfaced with a commercial 10G switch having both types of ports. As an alternative, a bi-directional interface was developed that can be used for such purpose. It is named GLAPPER to recall its functionality to be a transit between GLAss and coPPER.

In order to increase the instantaneous input bandwidth, an ADB3 Module has been defined. It is able to support 2048 MHz input bandwidth with a 2.048 GHz sampling clock. Nyquist input bands possible are 10–2048 MHz and 2048–3500 MHz. The main use of this module is with a fixed tuned bands configuration for a significant sensitivity improvement. Prototypes of the ADB3 Module are available and fully debugged.

The Core3 board is an evolution of the present Core2 processing board. It is mainly devoted to very high demanding processing capabilities. It is planned to be used as a digital preprocessor for L2C polarization conversion, for VLBI2010 FT configurations with 1 or 2 GHz input bandwidth, and in applications such as a spectrometer with a very high number of channels. The hardware has been fully defined, and the boards are expected before the end of 2010. Firmware applications are already simulated and ready to be debugged in the real board.

4. HAT-Lab

HAT-Lab is a spin-off company supported by INAF for the DBBC production. The company has agreements with IRA-Noto, where laboratories are placed for a part of the production, and MPI in Bonn where other phases of the production are realized. A certain number of operations are realized by external specialized companies to simplify and optimize the production of the complex boards. Assembly and testing is fully realized in HAT-Lab, IRA, and MPI.

At present eight systems have been deployed by IRA, and HAT-Lab is going to deliver eight additional systems. In the second half of 2010, the same number of units are expected to be produced. The production capability of HAT-Lab is around twelve systems per year, and production time is close to six months.

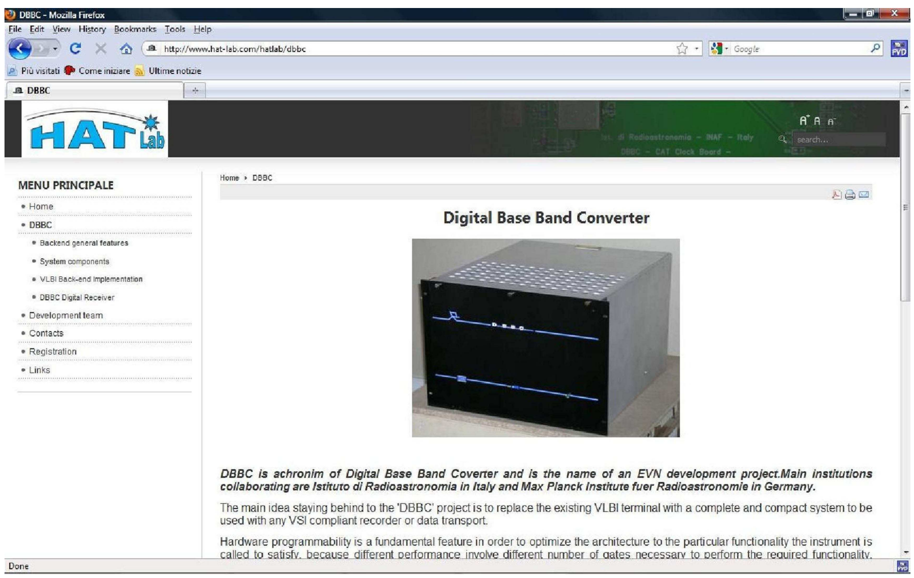

Figure 1. HAT-Lab Web site.