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The Progress of CDAS

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Abstract

The Chinese Data Acquisition System (CDAS) based on FPGA techniques has been developed in China for the purpose of replacing the traditional analog baseband converter. CDAS is a high speed data acquisition and processing system with 1024 Msps sample rate for 512M bandwidth input and up to 16 channels (both USB and LSB) output with VSI interface compatible. The instrument is a flexible environment which can be updated easily. In this paper, the construction, the performance, the experiment results, and the future plans of CDAS will be reported.

1. Introduction

In China, VLBI technology has been applied to orbit monitoring and orbit determination of spacecraft. Several radio telescopes have been established, such as the 50m antenna in Beijing and the 40m antenna in Kunming. Additionally, another 65m antenna is under construction in Shanghai. Including the two 25m antennas built earlier in Shanghai and Urumqi, there are four antennas now, and five or more will serve in the future as the VLBI network in China.

With the development of digital techniques, traditional VLBI terminals will be replaced by digital ones. The need for such replacement is well known and motivated by the necessity of both renewing an obsolete system whose components' replacement is every day more difficult and of achieving better performance making use of more predictable digital techniques [1].

Nowadays, high performance ADCs and high performance FPGAs are widely used. They can also meet the requirements of VLBI digital terminals, which would be economically convenient, and they are flexible and of high resolution.

2. The Overview of CDAS

CDAS is the abbreviation of Chinese Data Acquisition System. The concept of CDAS is shown in Figure 1. CDAS has:

- 1024 MHz sampling rate per channel;
- Up to 4 IFs input and 16 channels output;
- 32MHz/16MHz/8MHz/4MHz/2MHz/1MHz bandwidth output selectable; and
- 1/2/4 or 8-bit sampling selectable Mark IV or VSI-H interface compatible.

CDAS has about 20dBm dynamic range of input power level from -44dBm to -4dBm with analog AGC. As Figure 2 shows, for each IF, there are one ADC and four FPGAs used for data processing including DDS, down conversion, and filtering. And in order to fit for tracking

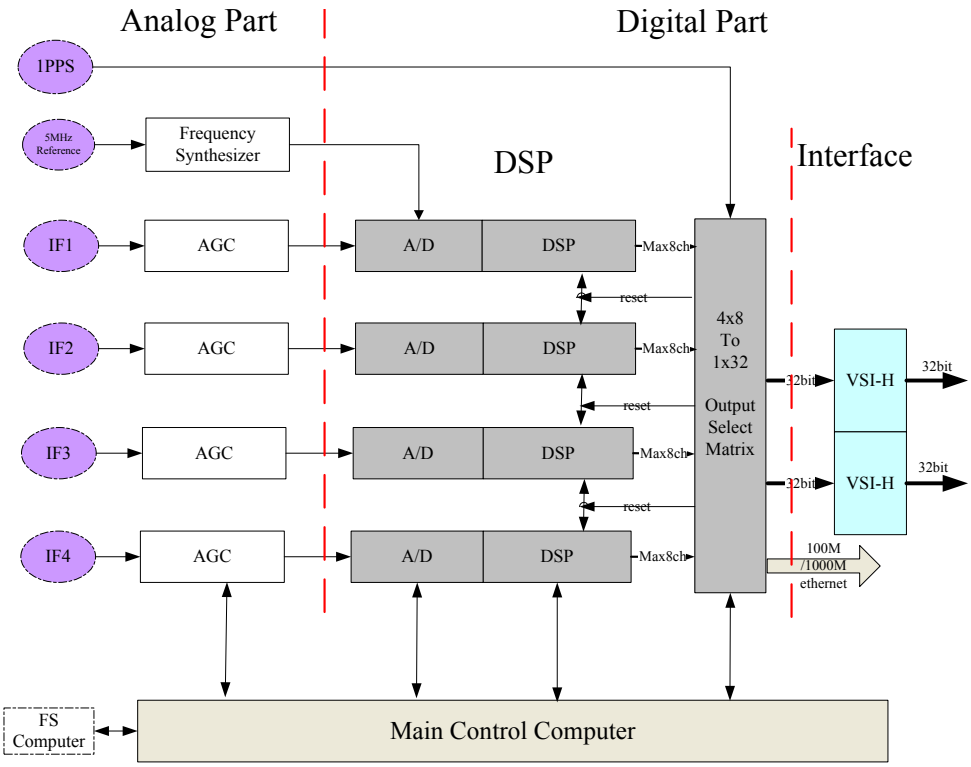

Figure 1. The concept of CDAS.

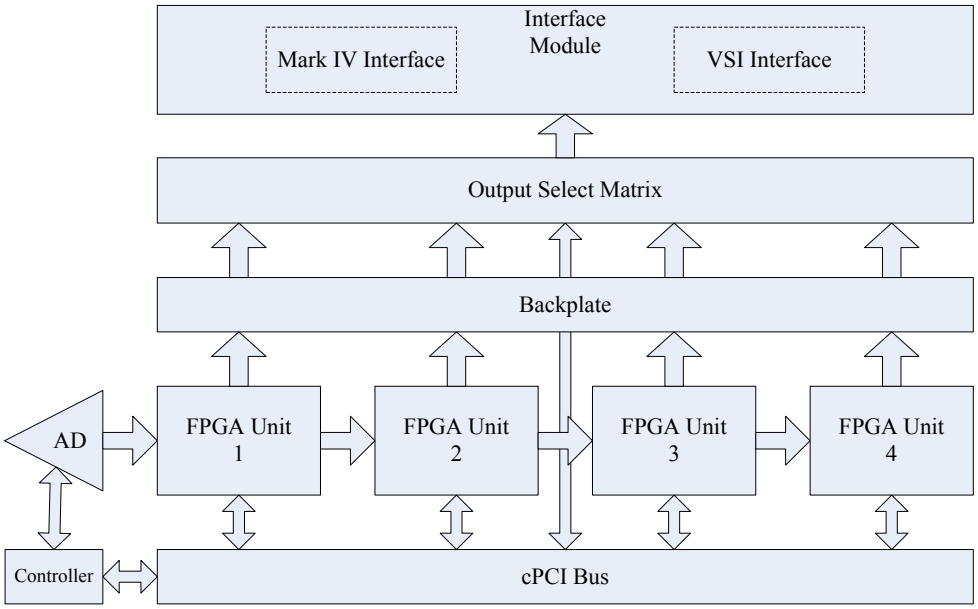

Figure 2. Signal Process Diagram.

spacecraft, the power level is calculated in each channel in order to avoid overflow. Each FPGA can produce one BBC including both USB and LSB. Another FPGA with PPC440 embedded is responsible for control and communication including cPCI bus control and communication with the Master Control Computer. The output select matrix module will select signals from the back plate and send them to the interface. The interface can be connected to a Mark IV formatter or a Mark 5B VSI-H interface.

3. Observation Results Comparison

Some comparisons between analog BBC (ABBC) and CDAS are shown below:

Figure 3 shows the result of a zero baseline test. The utilization of bandwidth is from about 75% (ABBC) up to 95% (CDAS).

Figure 4 shows the SNR comparison of a long baseline experiment between Shanghai and Kunming on 6 September 2009. The SNR of CDAS is much better than ABBC.

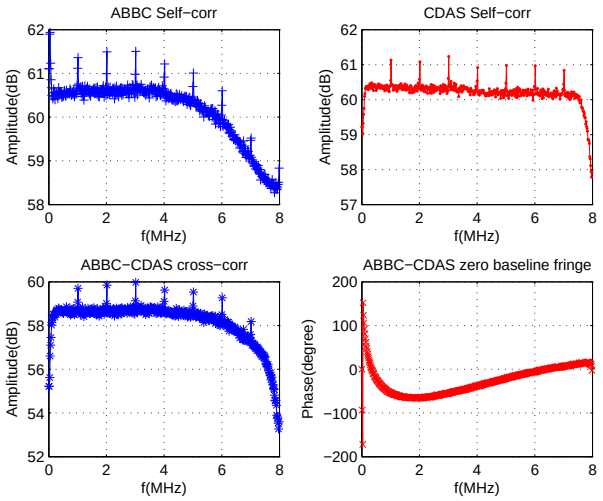

Figure 3. Bandwidth Comparison.

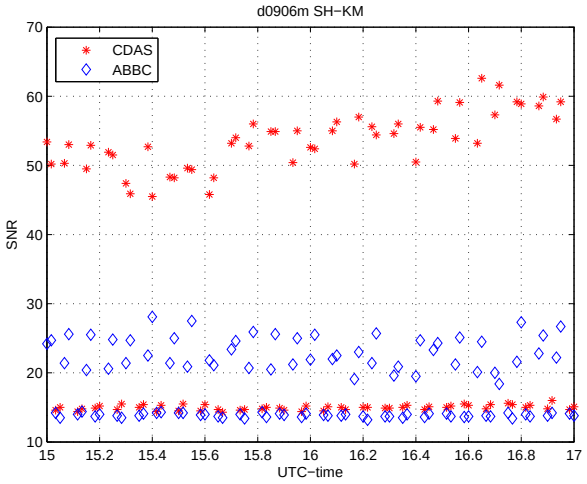

Figure 4. SNR Comparison.

4. CDAS at the Stations

Since January 2008, CDAS has been installed at Shanghai, Beijing, Kunming, and Urumqi—four VLBI stations. Figures 5 and 6 show the whole CDAS system at the Urumqi and Kunming stations, including FS Computer, Mark 5B, and LCD monitor.

After that, firmware and software have been updated several times during the past two years. CDAS will be applied in Chinese lunar projects in the future.

5. Future Plans

The sample rate of ADC is increasing from 1024 Msps to 2048 Msps, and this will double the total bandwidth of CDAS.

Figure 5. CDAS in Urumqi.

Figure 6. CDAS in Kunming.

10GigE and VDIF will also be supported to be compatible with Mark 5C in the future.

References

[1] Gino Tuccari, INAF-IRA In: IVS 2004 General Meeting Proceedings, pp. 234–237.