Next-Generation A/D Sampler ADS3000+ for VLBI2010

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⑤ Summary

Next-generation A/D ADS3000+

- AD chip
  - Sample analog signal up to 4 Gsps X 1ch
  - 2 Gsps x 2 ch, 1 Gsps x 4 ch available
- FPGA
  - Simple suppressing RFI signals (CW)
  - DBBC

Front panel

LCD Display

Status in LED

Control SW

Back panel

VSI out × 4

RS232C

Ethernet

Inside

A/D e2V
8bit,4,096MHz

FPGA
Xilinx Virtex5
XC5VLX110

FPGA
Xilinx Virtex5
XC5VLX220

ADS3000+,More Detail

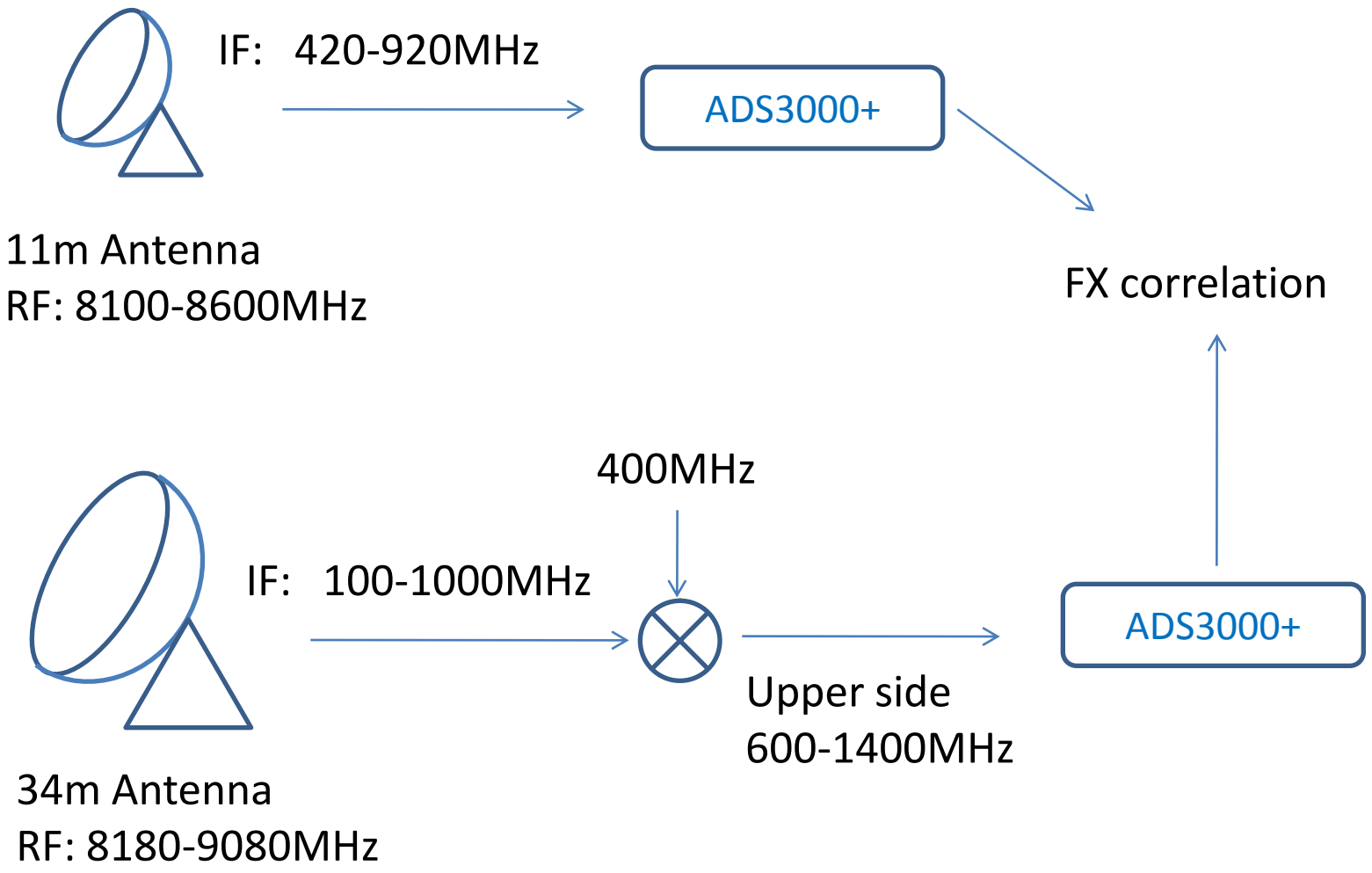
- test vector generater(TVG)
- timing adjustment with 1PPS
- Digital offset and gain control

Standard Sample Mode (to VSI)

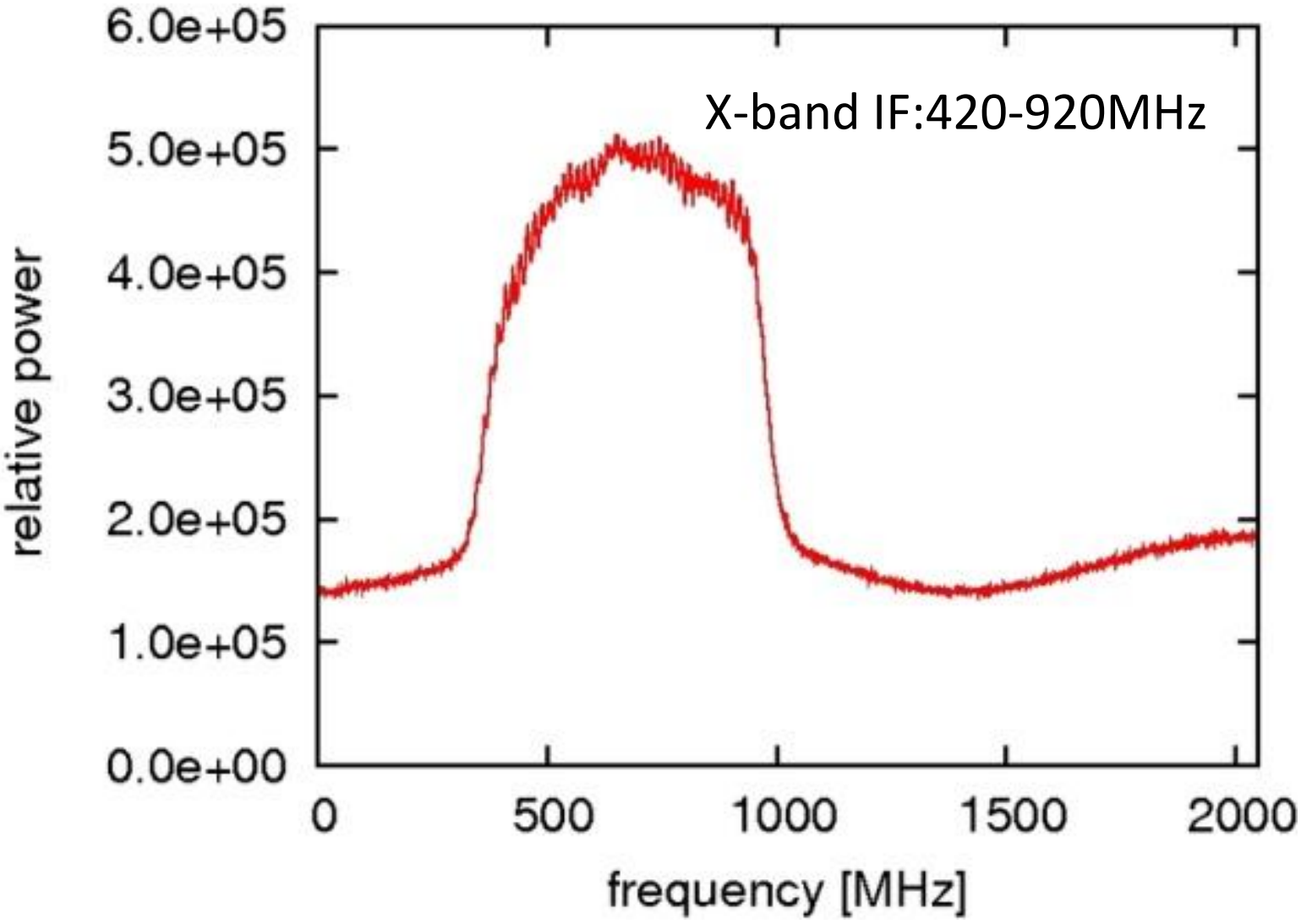
Mode	Rate	Quantization	Record
A	128Msps	8bit	1Gbps
B	1024Msps	2bit	2Gbps
C	512Msps	4bit	2Gbps
D	2048Msps	2bit	4Gbps
E	1024Msps	4bit	4Gbps
F	512Msps	8bit	4Gbps
G	4096 Msps	1bit	4Gbps

4GHz sampling fringe test

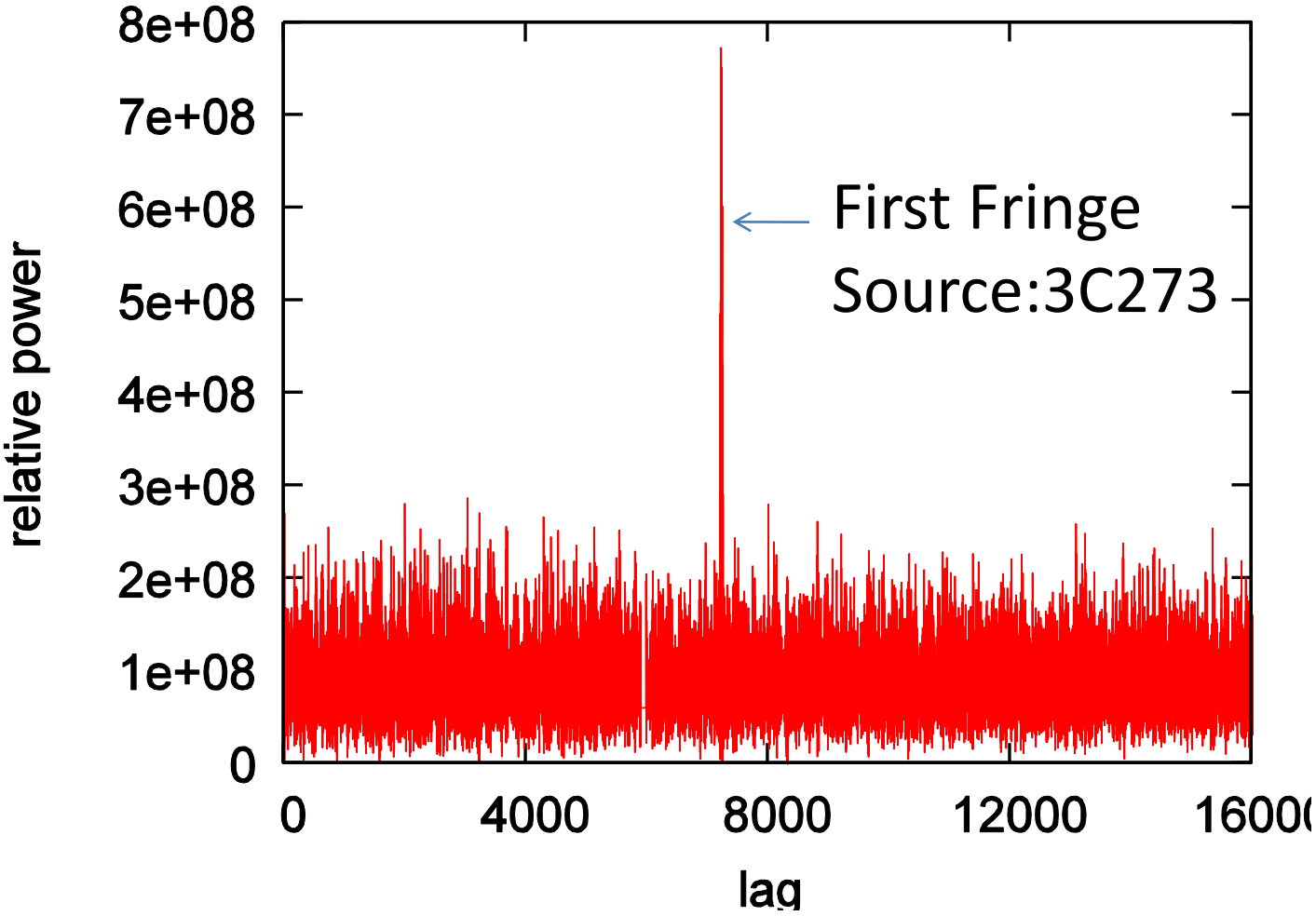
4Gsps Fringe Test



Band character of Kashima 11m



4Gsps First Fringe with ADS3000+



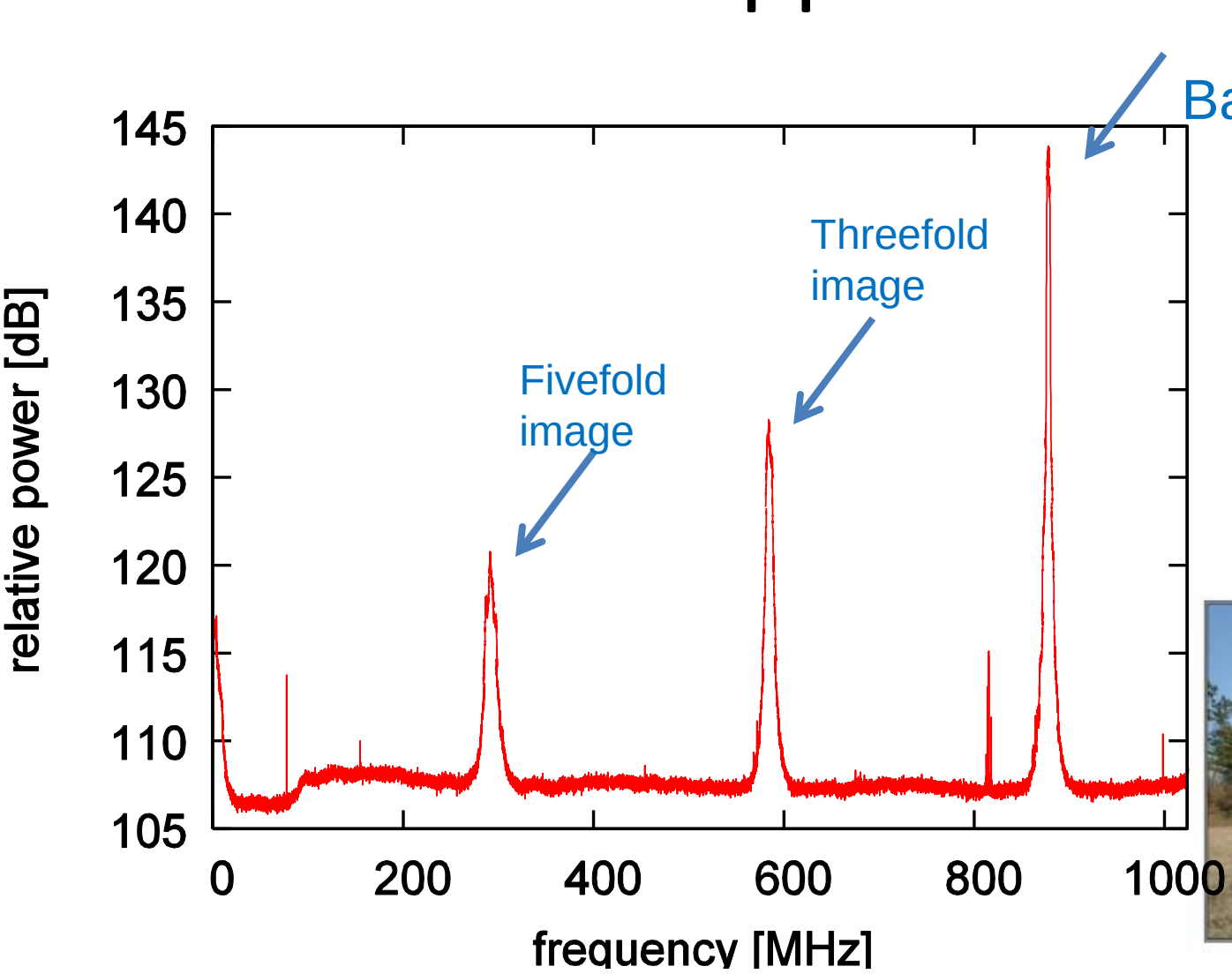
DSP with ADS3000+ FPGA

Real-time filtering

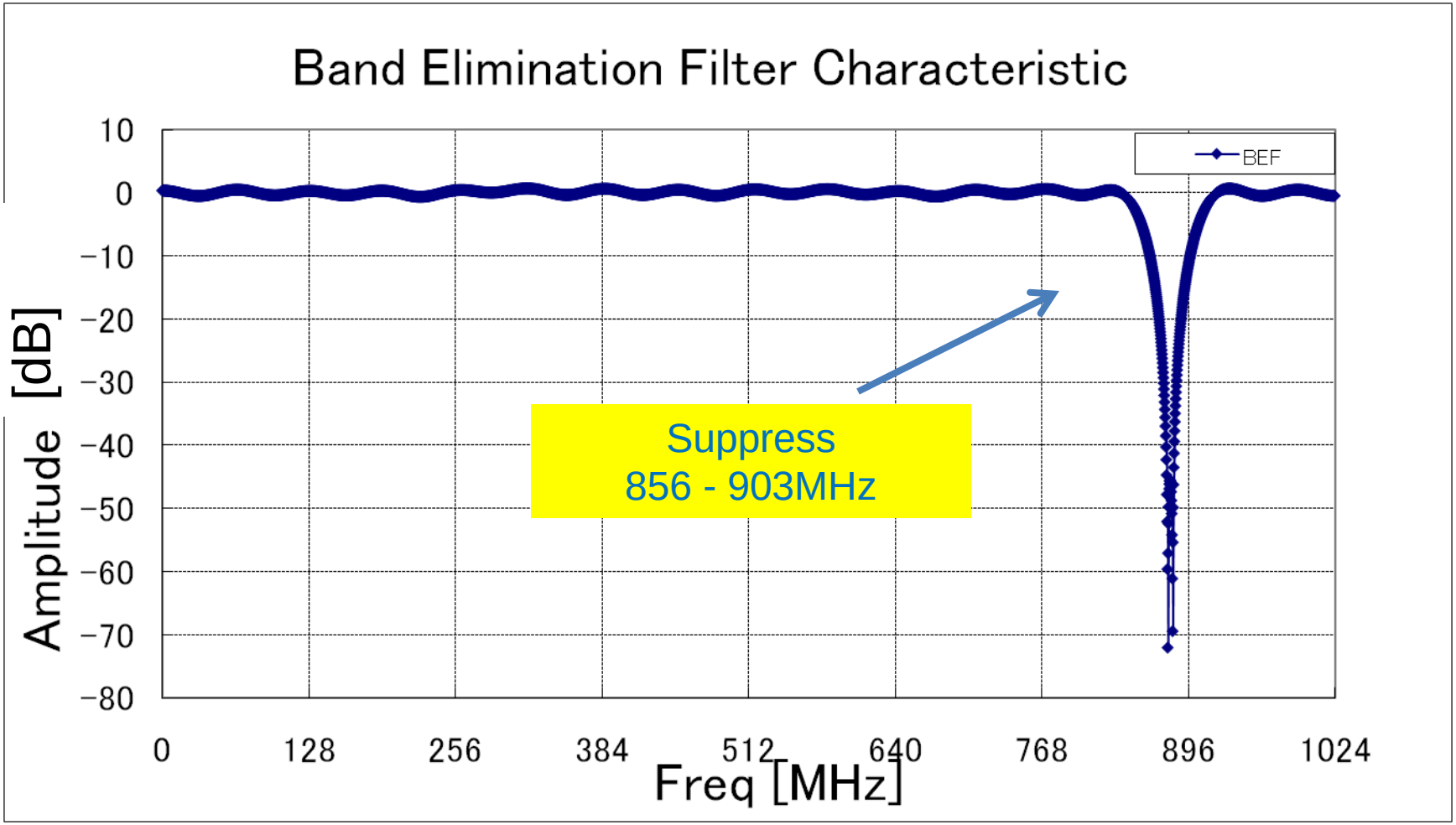
- Simple FIR filter
- Only at 2048Msps x 2ch
- 65 taps, 8bit filter is limited
- Any filter coefficients is possible to change
- MATLAB Filter coefficient (.fcf) is used

Ex: RFI suppression

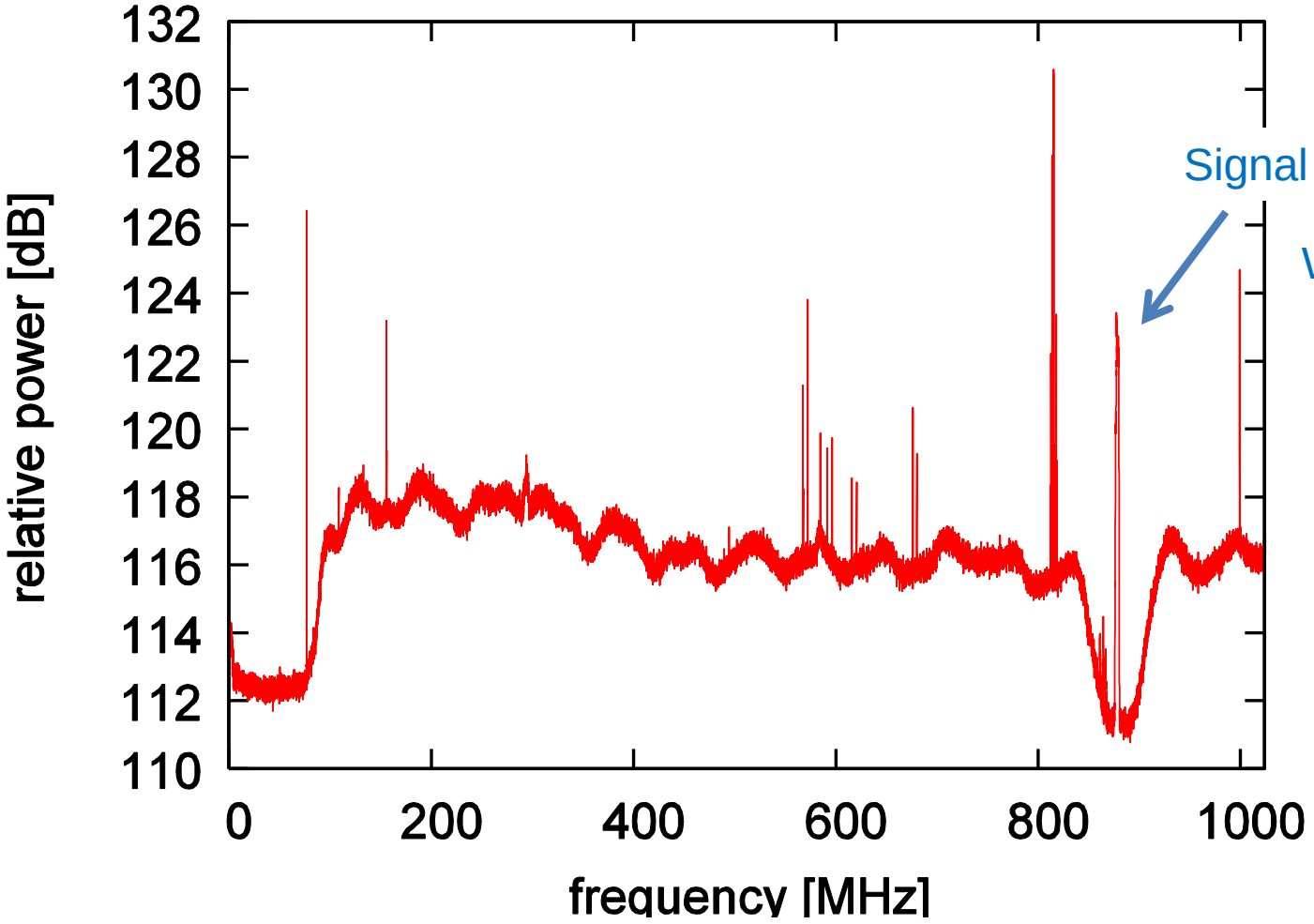
RFI suppression



Ex: Adopt Band Elimination Filter



After band elimination filter



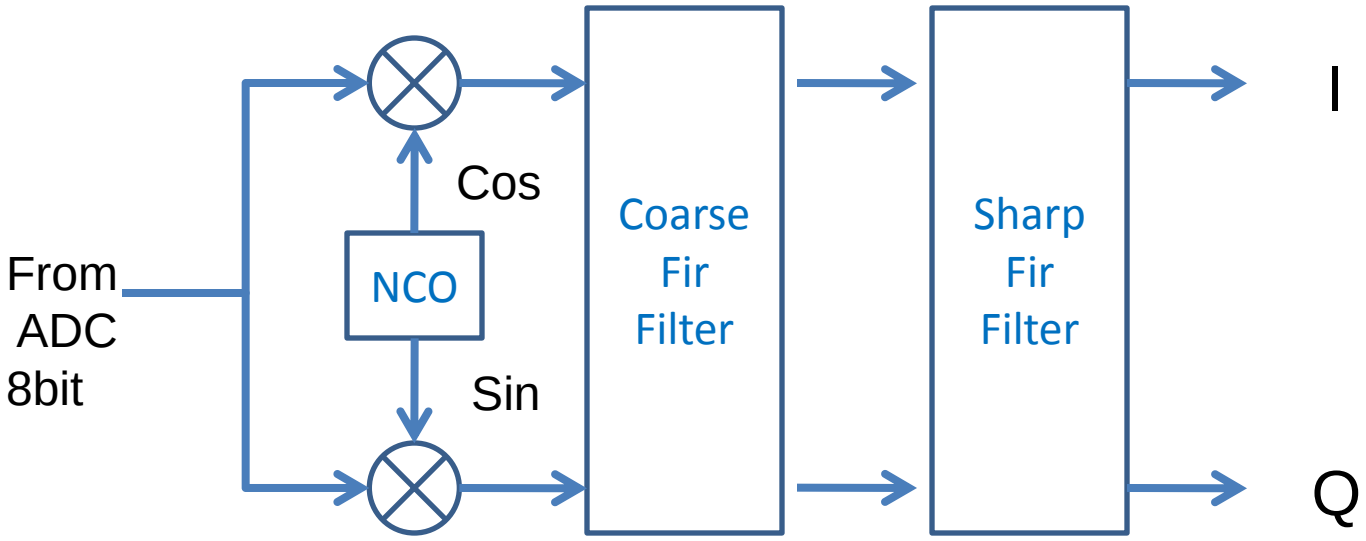
DBBC(Digital Base-Band Conversion)

- Base design is Weaver modulator
- Proto type 2ch DBBC property was evaluated
- New 16ch DBBC is under checking now
- We plan to perform 16ch DBBC fringe test soon

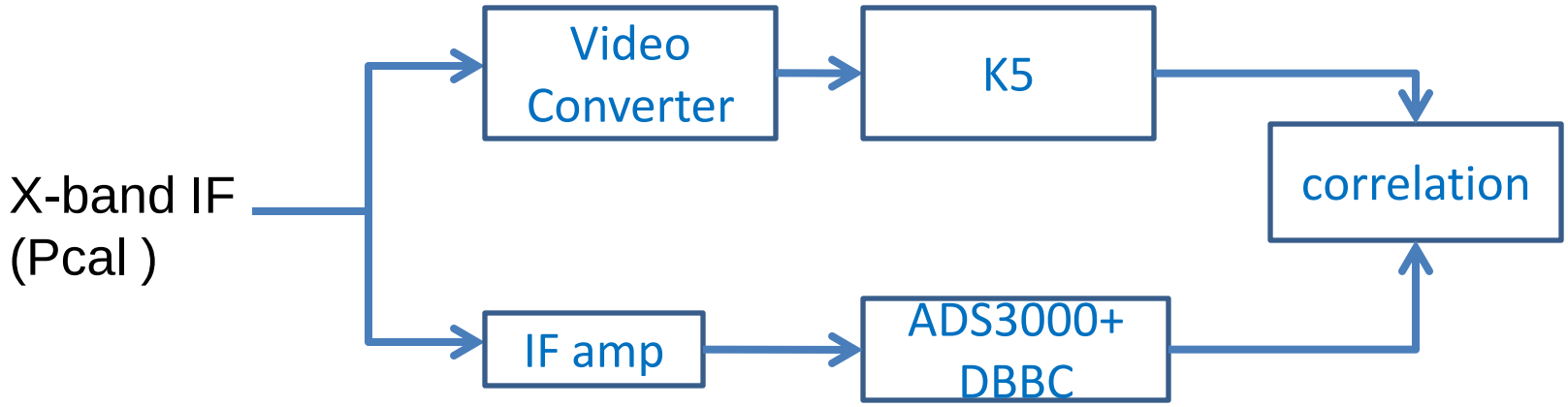
DBBC, More detail

- DBBC is performed @ 1Gsps x 4ch mode
- Bandwidth is extracted to 4,8,16,32MHz
- Output complex, USB, LSB are available
- 1Hz tune is possible in NCO(numerical control oscillator)
- NCO also controls angular acceleration

Proto type 2ch DBBC flow



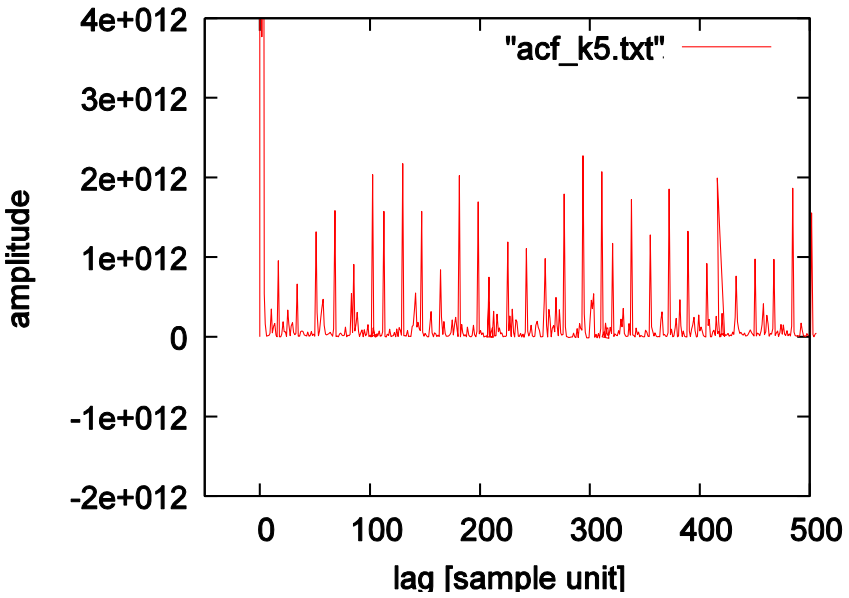
Zero baseline test with K5 sampler



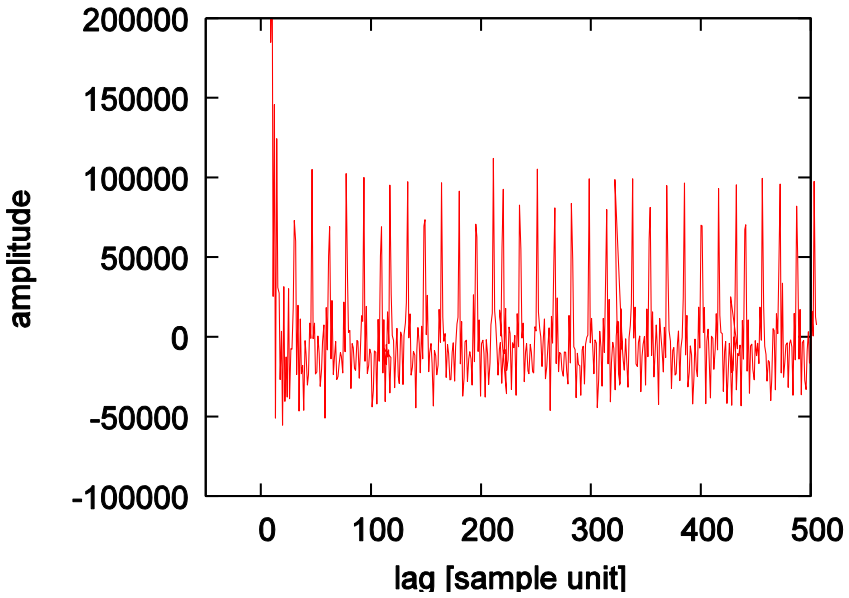
Both sampler sampled 16MHz,8bit

Auto-correlation K5 and DBBC

K5

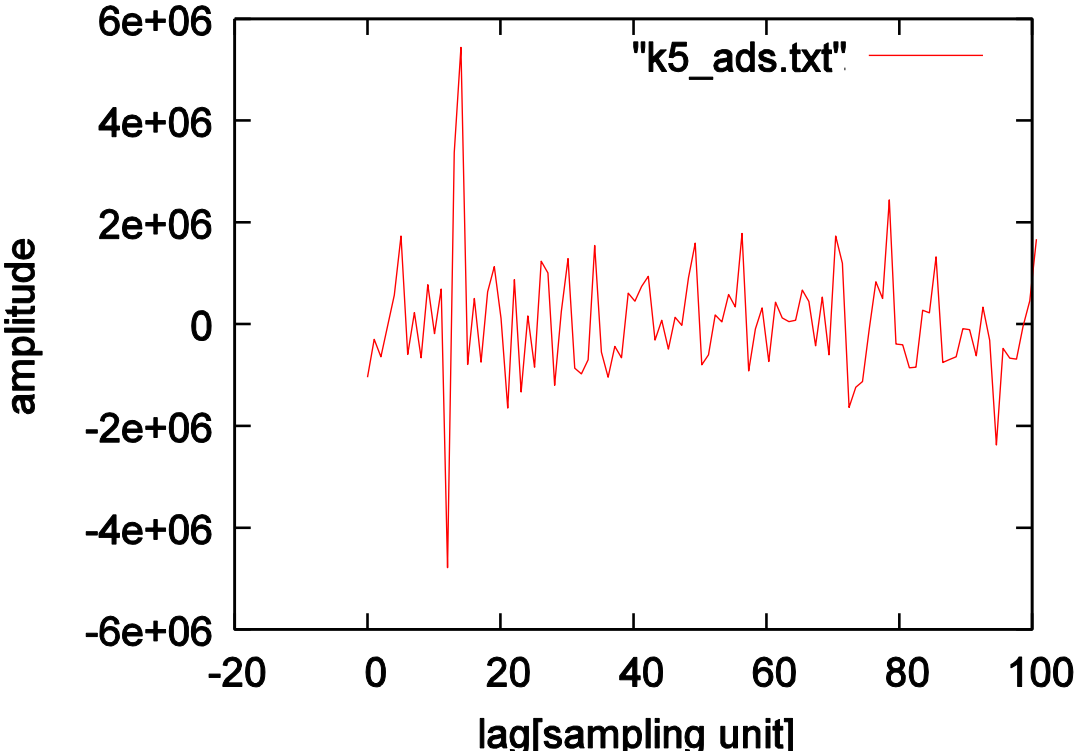


DBBC



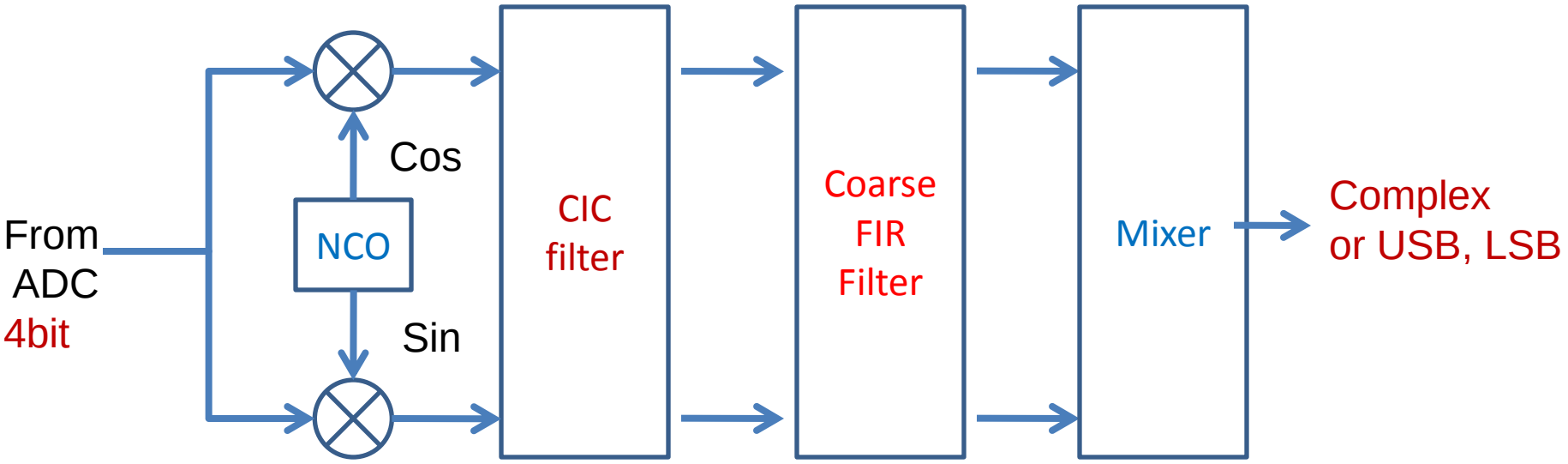
Pcal interval can be obtained
in both auto-correlations

Correlation between K5 and DBBC



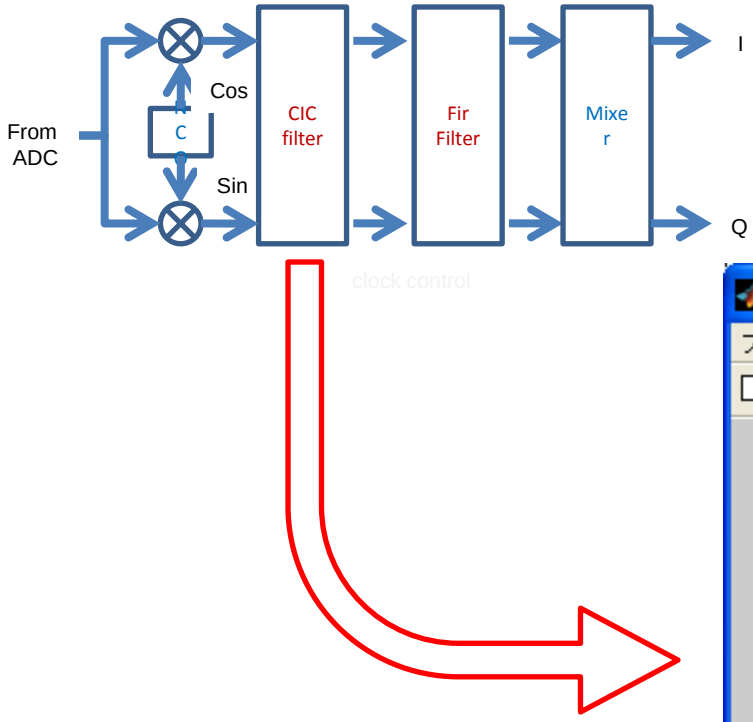
Successfully detected fringe
Peak is located 15 lags (16Msps), thus delay is about 1ns

New 16ch DBBC



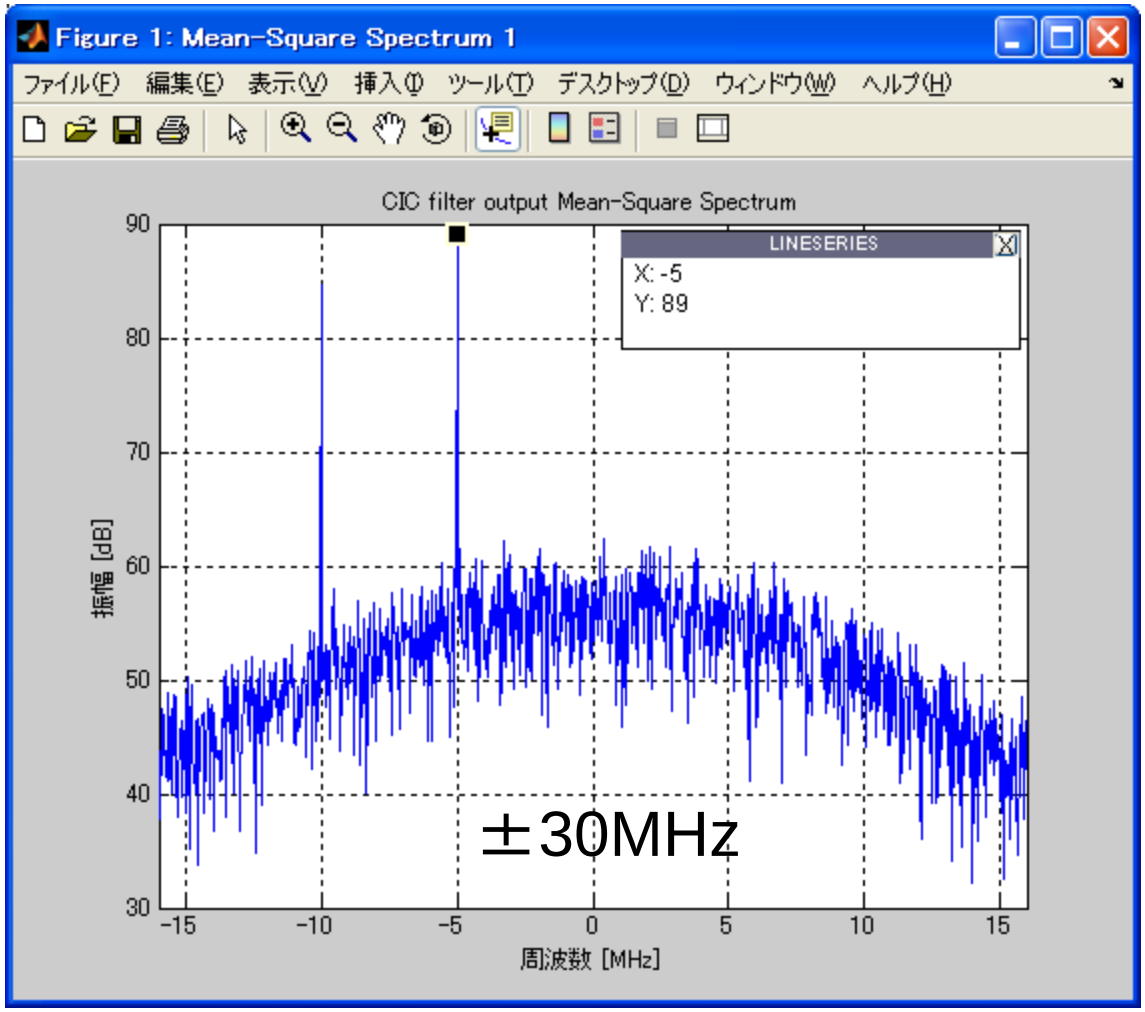
To fit into FPGA, CIC + FIR filter has been applied
CIC is cascade integrator comb, small circuit, but as LPF

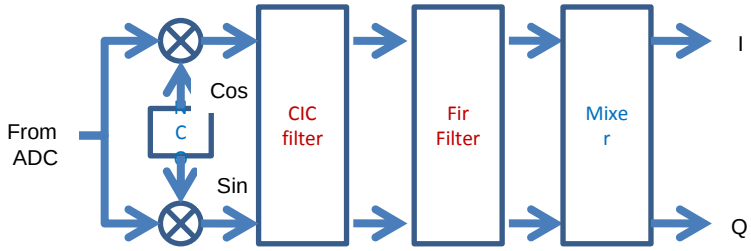
DBBC@32MHz

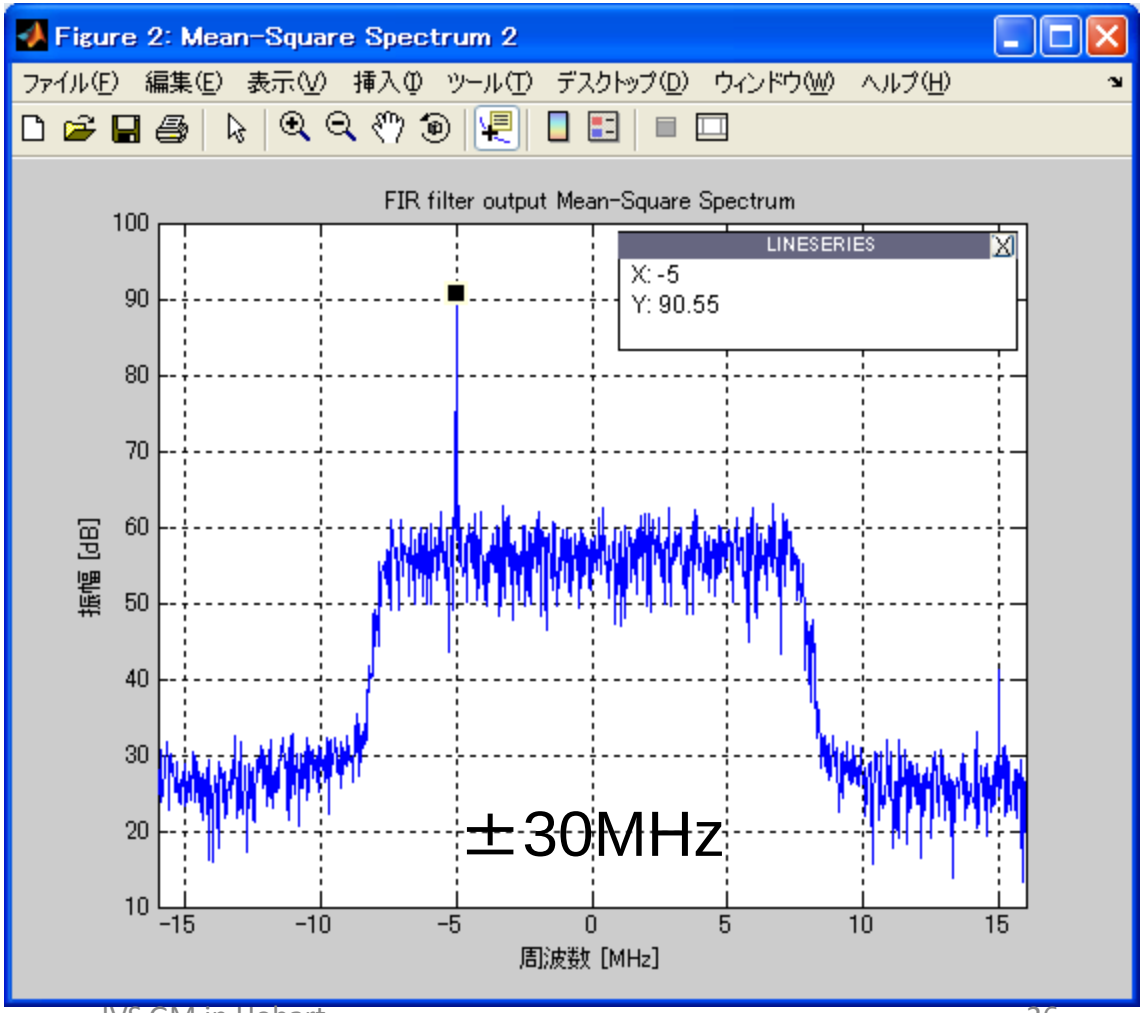


Input 10MHz and 20MHz

After CIC filter simulation result

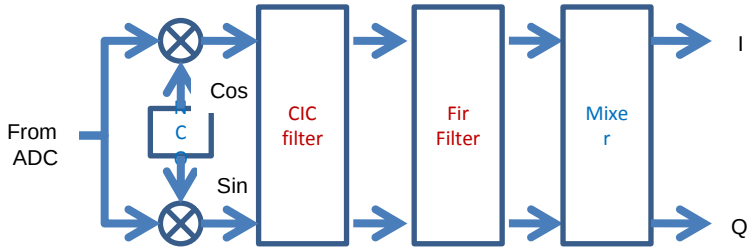




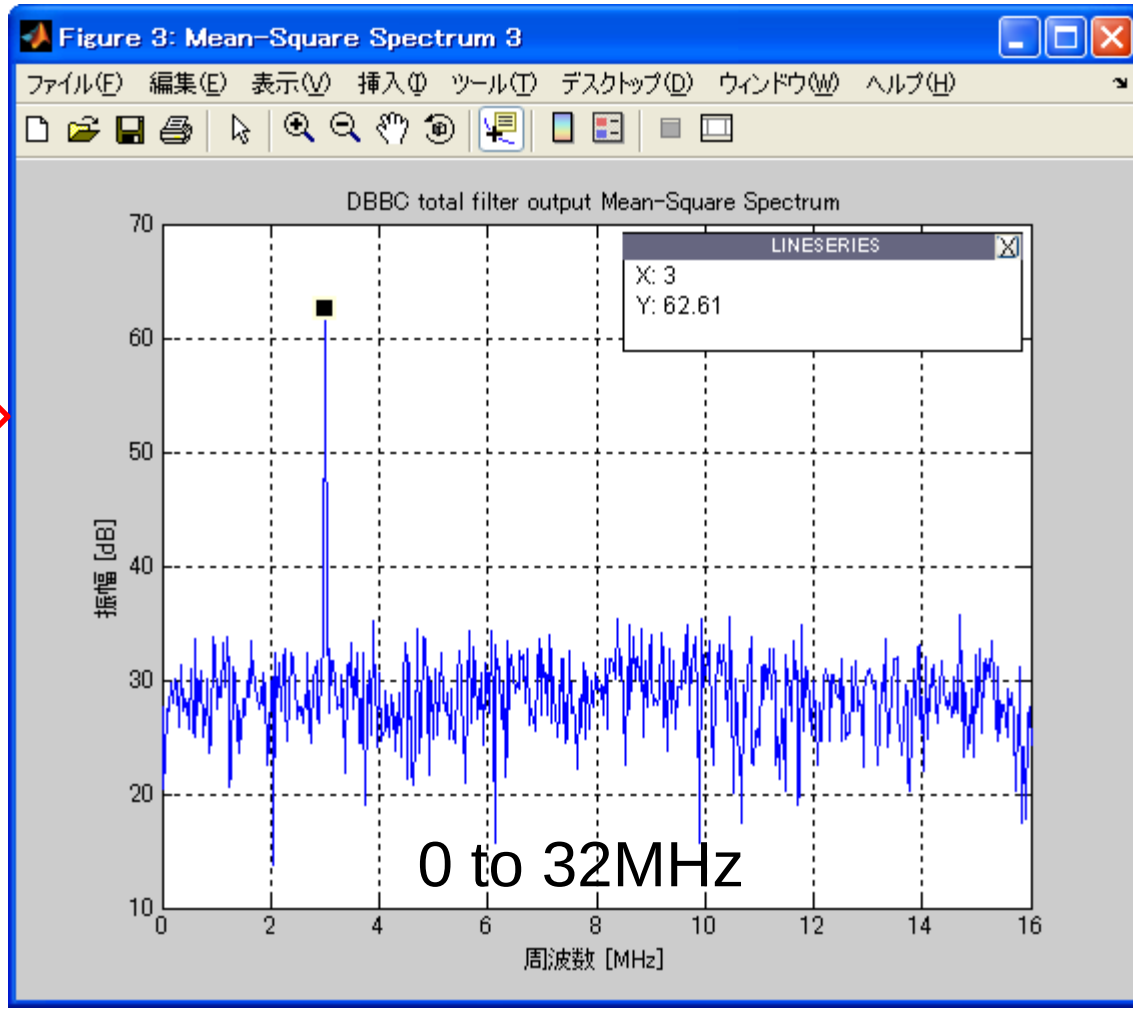


After FIR filter

CIC+FIR become sharp LPF



After Mixer
（in case of USB)



New 16ch DBBC

- To fit 16ch DBBC into FPGA capacity, filter changed from FIR+FIR to CIC+FIR.
- Complex and real output possible.

- Phase differences between 16ch are under checking.

Summary

- 4GHz fringe has been successfully detected
- real-time FIR filtering for RFI suppressing possible
- 16ch DBBC will be launch soon, after several test

And one more,

I am remaining of NICT speakers

Summarize NICT activities

NICT2010 for VLBI2010

MARBLE
Wide band receiver
System 2~10GHz

High speed
sampler
ADS3000+
4GHz and DBBC

GPU correlator
8stations @500Mbps

Ref signal

Optical fiber
round-trip
system
10^-17 / day
stability

KARAT and C5++
brand new software

Thank you very much for your attention!

Contact : takefuji@nict.go.jp

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