The Progress of CDAS
--Chinese Data Acquisition System

Renjie Zhu, XiuZhong Zhang, WenRen Wei, Ying Xiang, Bin Li, Yajun Wu, Fengchun Shu, Jintao Luo, Jinqing Wang, Zhuhe Xue, Rongbin Zhao, Lan Chen

Shanghai Astronomical Observatory, CAS

Outline

- Background
- Structure of CDAS
- Observation Results Comparison
- Future Plan

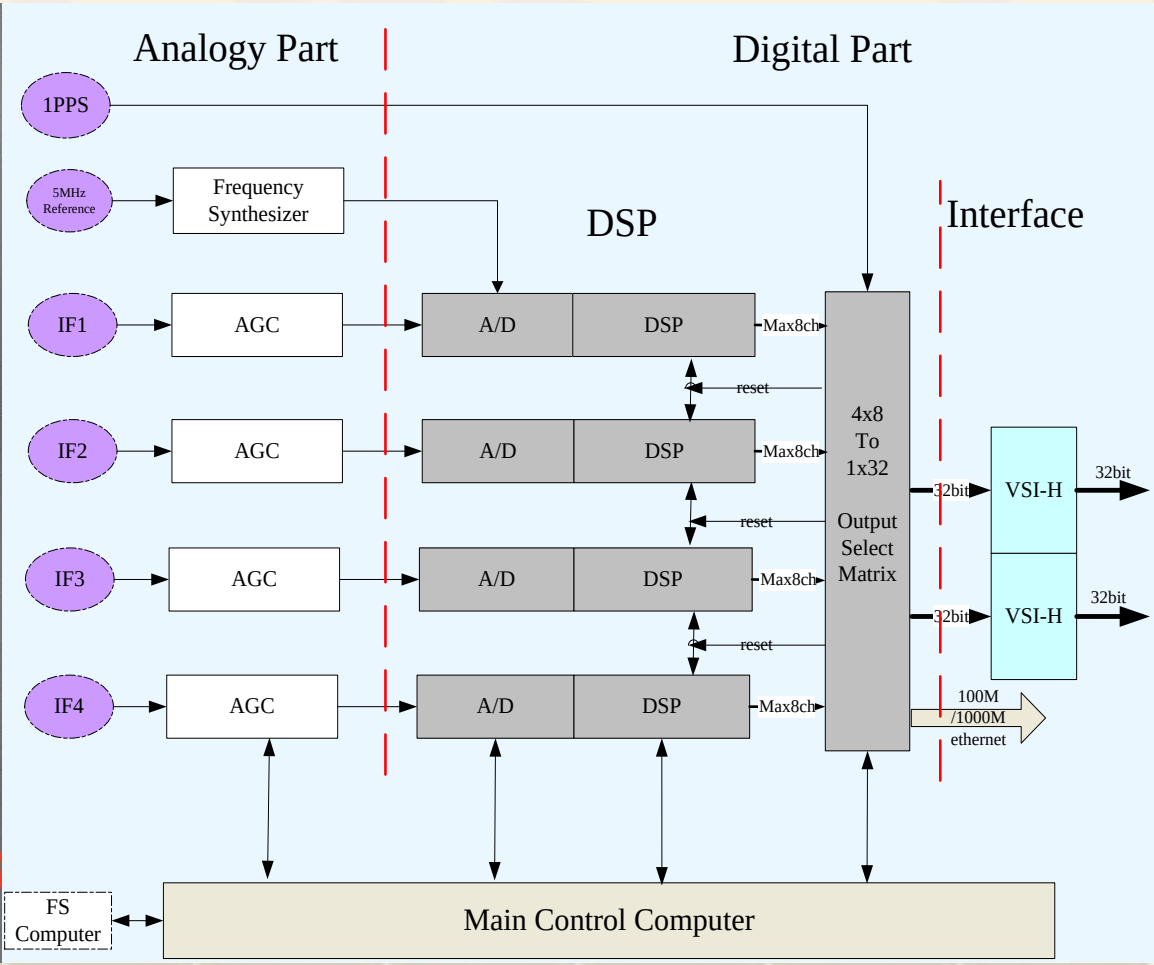
Background

- There are several stations established or under construction in China
  - Beijing 50m (finished)
  - Kunming 40m (finished)
  - Shanghai 65m (under construction)
- The traditional BBCs are difficult to upgrade or maintain
- DSP technology is rapidly developing and widely applied in many fields
  - High speed ADCs
  - High performance FPGAs

What is CDAS?

- CDAS: Chinese Data Acquisition System
- 1024MHz Sampling rate per channel
- Up to 4 IFs input and 16 channels output
- 32MHz\16MHz\8MHz\4MHz\2MHz\1 MHz bandwidth output selectable
- 1、 2、4 or 8-bit sampling selectable
- MK4 or VSI-H interface compatible

Structure of CDAS



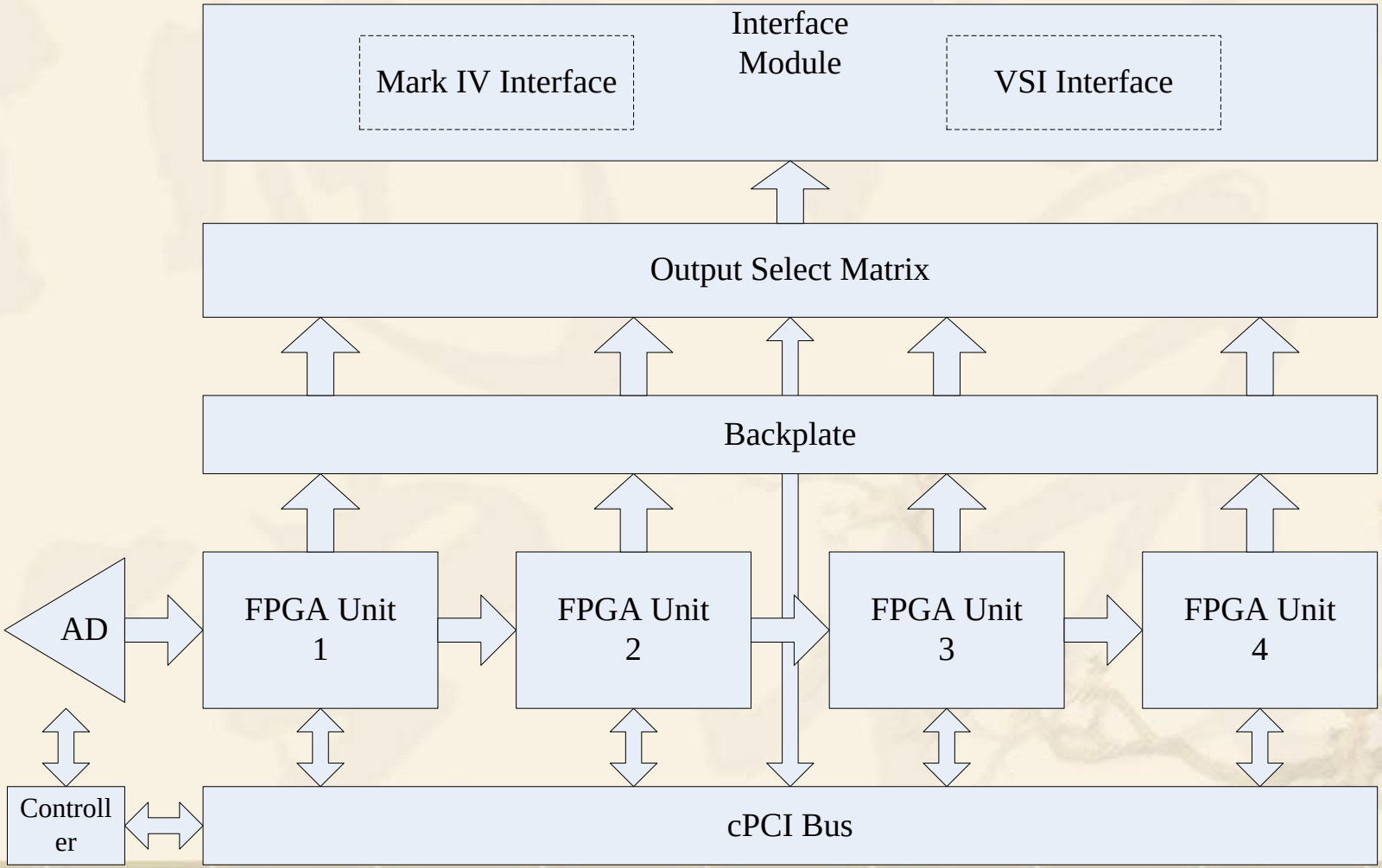
Analog Part

- Analog Part
  - Anti-aliasing filter:
    - LOW : 10MHz~512MHz
    - HIGH : 512MHz~1024MHz
  - AGC：
    - Input signal power: -24dBm±20dBm
    - Output signal power: 0dBm±0.5dBm
  - Frequency Synthesizer:
    - 1024MHz Sine wave
    - 0° and 180° in phase

Digital Part

- A/D Converter:
  - Dual ADC with 8-bit Resolution
  - 1024Msps sampling rate per channel
  - 2048Msps in Interlace mode supported (to be expanded)
- DSP components
  - Four FPGAs used for data process (dds, down convert, filter, sub-channel power calculation…)
  - Each FPGA can produce one BBC including both USB and LSB
  - Another FPGA used for control and communication (cPCI bus control, communication with MCC…)
- Output select matrix
  - Select signals from backplate for output
  - Mark IV & VSI-H interface

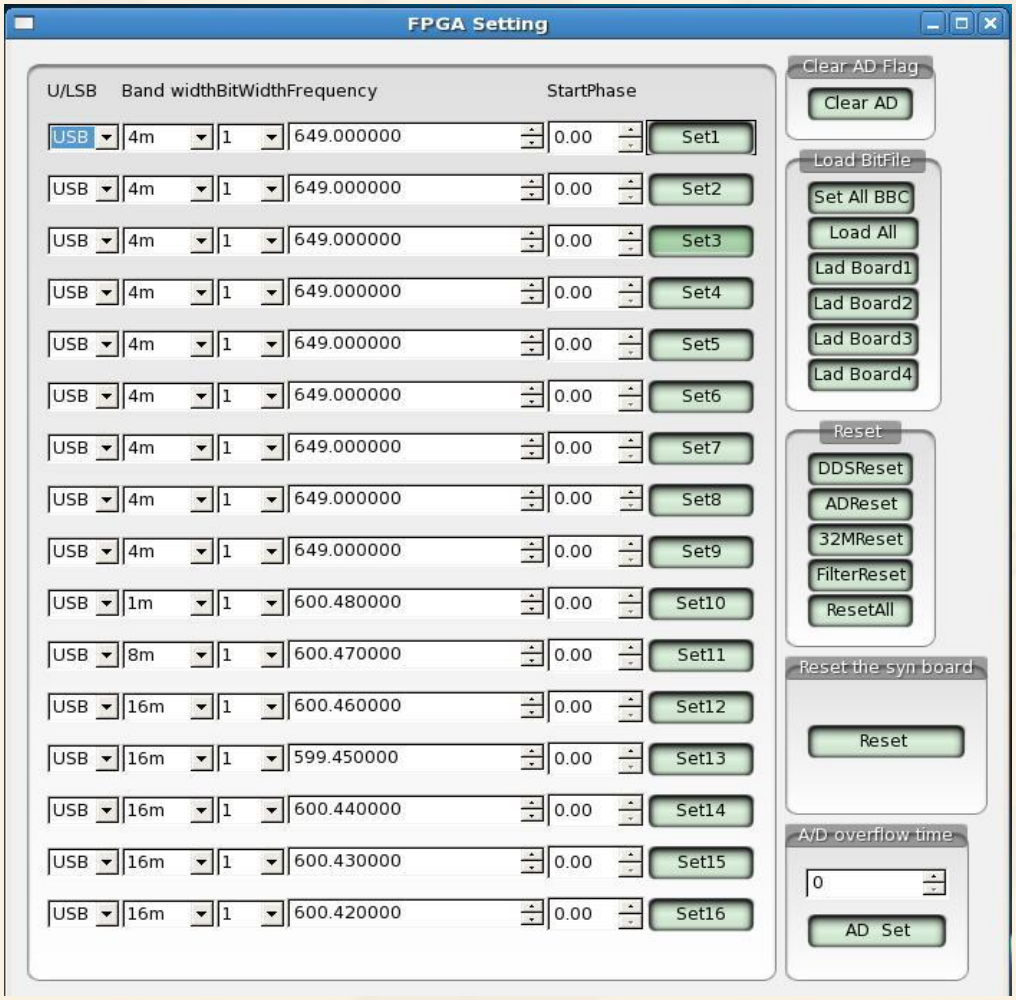
Data Flow Diagram



Main Control Computer

- cPCI-Bus based IPC (performance not so high but stable)
- System Initiate
  - FPGA downloading
  - Default parameter setting
- Parameter Setting GUI
- Status Monitor GUI
- Communicating with FS

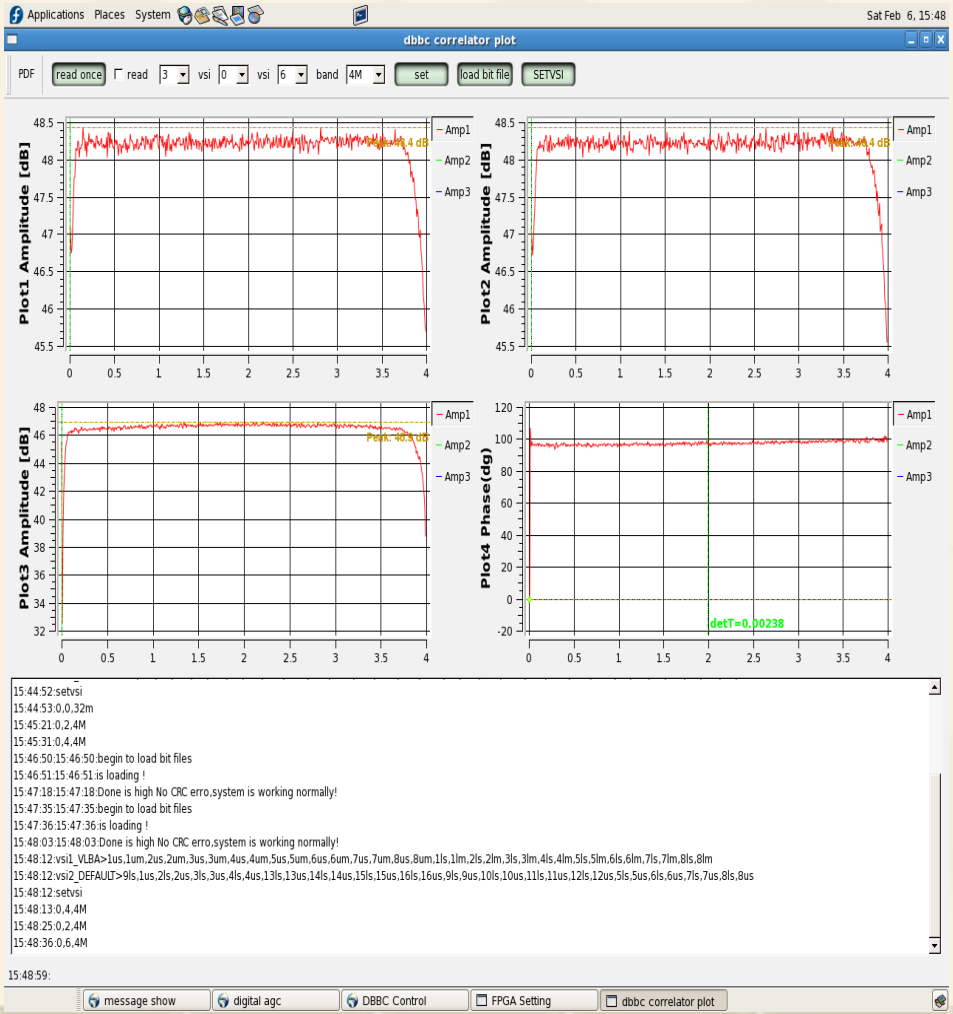
Parameters Setting GUI



- FPGA Downloading
- System Reset
- USB/LSB select
- Bandwidth setting
- DDS Frequency
- Initial phase of DDS

All of these can be achieved automatically under the control of FS computer.

Status Monitor GUI



- Self-correlate
- Cross-correlate
  - Amplitude
  - Phase

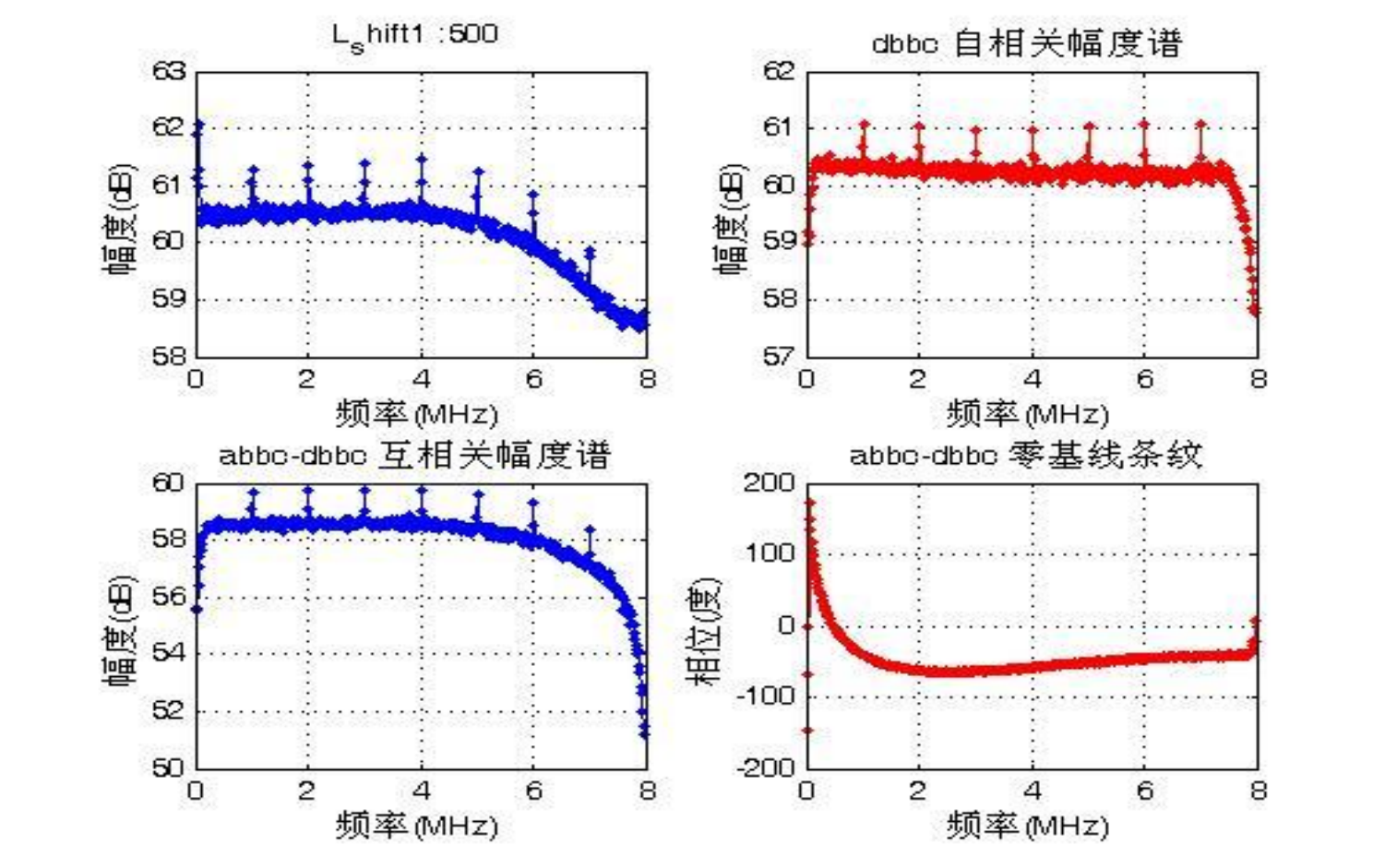
If there is anything abnormal during the observation, it can be recognized immediately on the screen.

Comparison

- Flatness In Band
- SNR
- Delay Residual

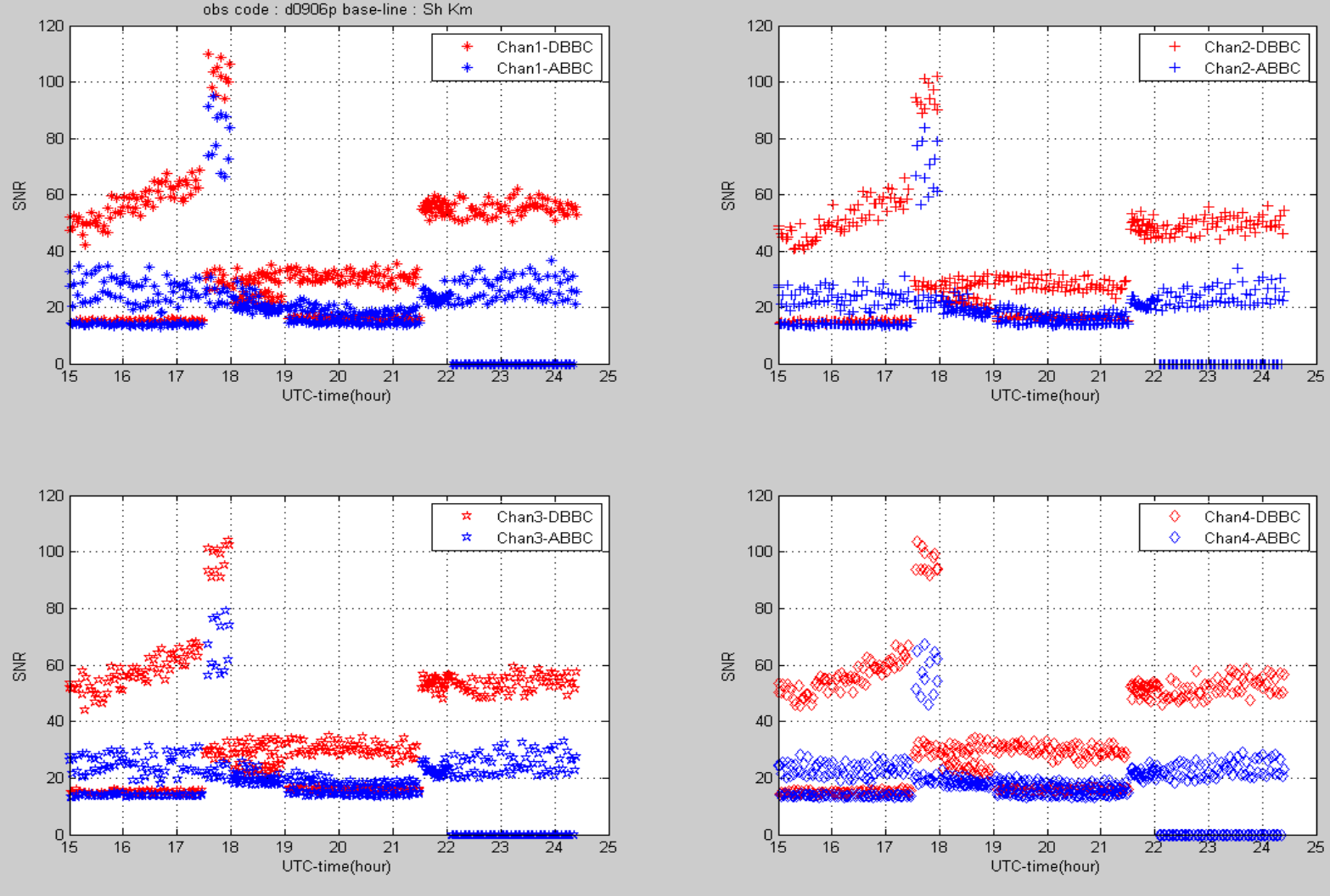
Pass band Comparison

(Zero baseline observation)



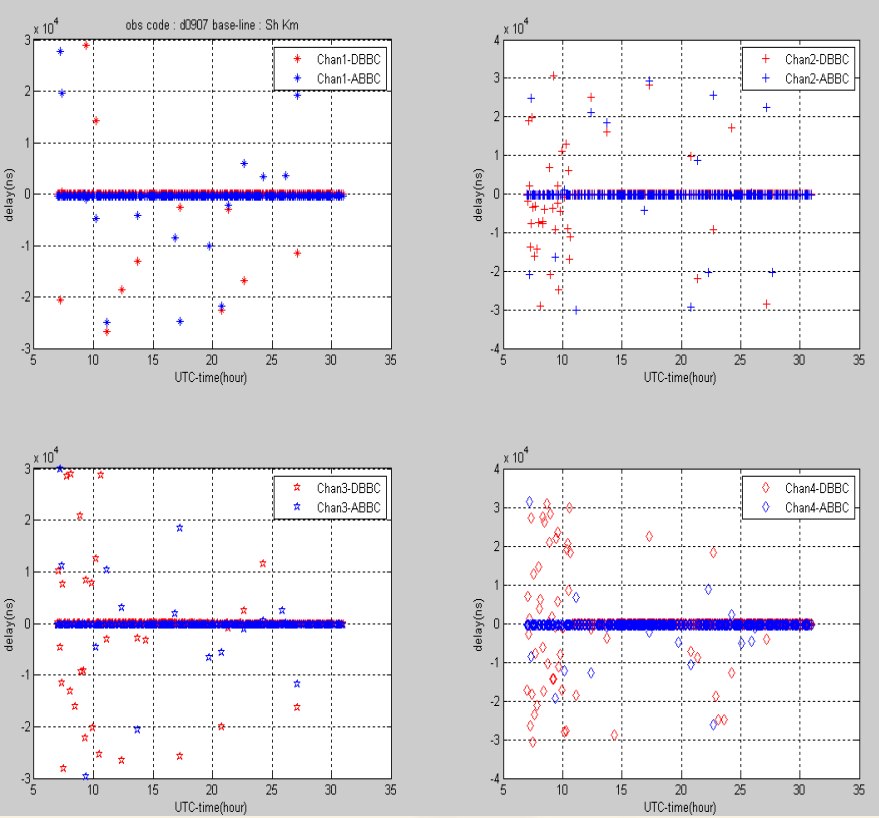
SNR Comparison

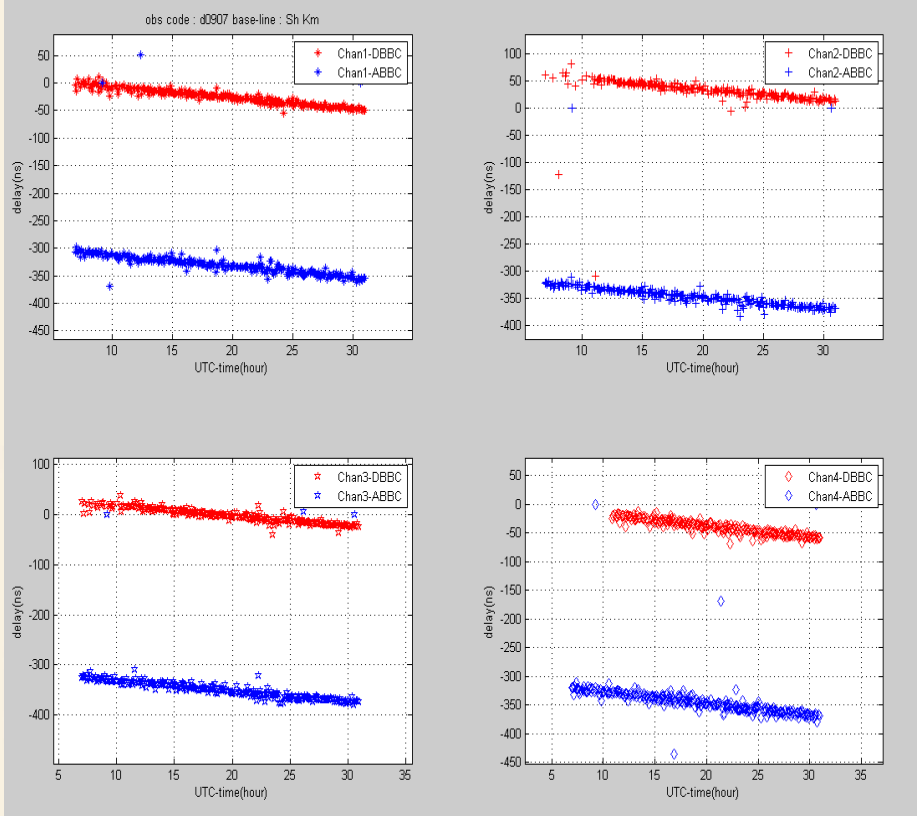
(Long baseline observation)



Delay Residual Comparison

(Long baseline observation)





CDAS in the Stations

- Since Jan,2008
- Firmware and software have been updated several times during two years
- Would be applied in Chinese Lunar Projects

Future Plans

- Expanded to 2Gsps or higher
- 10GigE Output
- VDIF Format

Thank you for your attention!