DBBC2 Setup and Operations

G. Tuccari
General Functionality

Antenna
Feed
LNA

Backend

Recorder
Network
Correlator
General Functionality

Backend Schematic Block

IF Band Forming → Base Band Forming → Stream10GE VDIF
DBBC2 /DBBC2010 General Features

• 4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz
• 1024/2048 MHz sampling clock frequency
• More personalities for different observing modes
• Input 4/8 polarizations / bands
• Output 4/8 groups of 32 data channel
• Output as VSI interfaces or as 10G Ethernet streams
• Control under Field System or other client console
DBBC
Hardware Structure
DBBC2 Architecture

IFn (MHz)
1~512, 512~1024, 1024~1536, 1536~2048
or
1~1024, 1024~2048 MHz

AGC/Filter

ADB 1/2

1024/2048 MHz Synthesizer Distributor

H-Maser

PCI Interfaces

PCI

FS PC

2 x 4 Gbps Glass/Copper

VSI 64 ch

FILA OUT

FILA 10G

IF 1abcd

IF 2abcd

IF 3abcd

IF 4abcd
DBBC2010 - Half VLBI2010 Compliant
8 IFs @ 512 MHz
Output data rate 16 Gbps

IFn (MHz)
1~512, 512~1024, 1024~1536, 1536~2048
DBBC2010 - Full VLBI2010 Compliant
8 IFs @ 1024 MHz
Output data rate 32 Gbps

IFn (MHz)
0~1024, 1024~2048, 2048~3072 MHz

H-Maser
1024/2048 MHz Synthesizer Distributor

FS PC
PCI PC
PCI Interfaces

4 x 8 Gbps Glass/Copper
DBBC2 / DCCB2010
Schematic Top View

STACK = ADB1/2 - Core2 (min 1 – max 8)
Review of the System Components

• Analog Conditioning Module - CoMo
• Analog-Digital Converter (ADB1 - ADB2)
• Data Processing (Core2)
• Connection and Service
  (FiLaIN/OUT – FiLa10G FILA10G-4)
• Timing and Clock (CaT2 – Clock and Timing)
• Computer Control (PCSet)
Conditioning Module (Unica3)

- 4 selectable RF input
- 4 selectable Nyquist Filters
- 31.5 dB Programmable Attenuation
- Total Power Full Band
- Manual or Automatic Gain Control
Conditioning Module (Unica4)

- 4 selectable RF input
- 8 selectable Nyquist Filters
- 31.5 dB Programmable Attenuation
- Total Power Full Band
- Manual or Automatic Gain Control
1 CoMo includes 2 Unica4
ADB1

Analog to Digital Converter

Analog input: 0 - 2.2 GHz
Max Sampling clock single board: 1.5 GHz
Max Instantaneous Bandwidth in Real Mode: 750 MHz
Max Instantaneous Bandwidth in Complex Mode: 1.5 GHz

Output Data: 2 x 8-bit @ 1/4 SClk DDR
ADB2

Analog to Digital Converter

Analog input: 0 – 3.5 GHz

Max Sampling clock single board: 2.2 GHz

Max Instantaneous Bandwidth in Real Mode: 1.1 GHz

Max Instantaneous Bandwidth in Complex Mode: 2.2 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR
4 x 8-bit @ 1/8 SClk DDR

Piggy-back module support for 10-bit output and connection with FiLa10G board.
Core2

Basic processing unit

Input Rate:
(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s
(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s
More...

Typical Output Rate:
(64 ch x 32-64-128) Mb/s

Programmable architecture

Es. Digital Down Converter:
1 Core2 = 4 BBC
1 Core2 = 1 Polyphase 16 Filter Bank

1 VSI 32 ch output in piggy-back
FiLa Board IN/OUT

First and Last board in the stack

First:
Communication Interface
JTAG Programming Channel
1PPS Input

Last:
2 VSI Interfaces
1PPS Monitor Out
80Hz Continuous Cal Out
PCSet

ADLink PCI9111HR: Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control, etc.

ADLink PCI7200: Communication with 32-bit bus for Core2 register setting, total power measurement, state statistics, etc.

Adventech PCI-7030: Half Size PCI Motherboard (Intel Atom) on PCI backplane

Xilinx programmer: FPGA device configuration through USB – JTAG interface
DBBC2 Module Stack
DBBC Box: air-flow path

The air cooling flow from a side view
How the DBBC is to be connected in your control room

- 10 MHz
- H-Maser 1PPS
- 1PPS test out
- 80 Hz cont cal
- RF/IF input
- VSI-H
- Monitor keyboard mouse network

Diagram showing connections in the control room.
FiLa10G

10G Optical Fiber Ethernet Board

- Triangle connection between HSI (DBBC fast sampled data bus) – VSI – 10Gb link

- It can be placed either at the beginning or at the end of the stack chain → 10G link / MK5C

- Piggy-back board for ADB2
FILA10G main features

- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 Gbps each 10G port
- Format mode: MK5B in two 5008 bytes packets
  - VDIF-ST in any allowed packet size
  - VDIF-MT corner turned under development in any allowed packet size
FILA10G and ADB2
FILA10G - SA
Connection examples

- 2 x VSI --> MK5C & 10GE net
  
  ![Diagram](image)

- 2 x VSI --> MK5C = MK5B & 10GE net
  
  ![Diagram](image)
Connection examples

• 2 x VSI --> Network

2 x VSI --> FILA10G --> 10 Gbps e-VLBI

8 x VSI --> FILA10G --> 2 - 4 - 8 - 16 - 32 Gbps

8 x VSI --> FILA10G - 4 --> 2 - 4 - 8 - 16 - 32 Gbps
Observing Modes
Observing Modes (today)

• **DDC**: tunable, channel bandwidth between 1 MHz and 16 MHz, U&L, Continuous cal with 80 Hz synchronization, mode ‘geo’, ’astro’, astro2, ‘w-astro’, ‘lba’, ’test’

• **PFB**: fixed tuning, channel bandwidth 32/64 MHz, all U or L depending on the Nyquist zone

• **DSC**: full 4 x 512/1024 MHz, max 8 x 1024 MHz band direct sampling conversion, all U or L depending on the Nyquist zone

• **SPECTRA**: 4Kch/IF spectrometer, max 32K channels
DDC - Digital Down Conversion to Base Band of Independent Channels
PFB – Polyphase Filter Bank

Conversion to Base Band, Fixed Band

Diagram showing the conversion process from high-band frequency to base band with binary data.
PFB – Polyphase Filter Bank
USB / LSB depends on the Nyquist zone

Nyquist zone 1 / 3

USB 1
USB 2
USB
USB
USB
USB
USB
USB 16

0 MHz
1024 MHz
512 MHz
1536 MHz

Nyquist zone 2 / 4

LSB 16
LSB
LSB
LSB
LSB
LSB
LSB 2
LSB 1

1024 MHz
2048 MHz
512 MHz
1536 MHz
DSC – Direct Single band Conversion Conversion to Base Band, Full Band
DSC – Direct Single band Conversion
USB / LSB depends on the Nyquist zone

Nyquist zone 1 / 3
USB

0 MHz
512 MHz
1024 MHz
1536 MHz

Nyquist zone 2 / 4
LSB

1024 MHz
2048 MHz
512 MHz
1536 MHz
How the observing mode is selected

- Using a dedicated firmware
- Using a dedicated control software
- Using a dedicated configuration text file
Welcome to the Hat-Lab home page

HAT-Lab s.r.l. is a INAF (Istituto Nazionale di Astrofisica) spin-off company.

The first and main goal is to produce and continue the development of the DBBC (Digital Base Band Converter) system, a digital back-end endorsed by the European VLBI network, and adopted as digital processing unit in the radiotelescopes worldwide for scientific research.

Indeed the system is a very flexible environment used to observe astronomic, geodetic and space science targets with interferometric or single-dish methods.

The wide band and high data rate processing of the DBBC allows to significantly improve the radiotelescope sensitivity and perform high precision data handling for a more accurate scientific result.
## Downloads

### Overview

Number of Categories: 6

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Files Structure
(under Windows XP)

- C:\DBBC\bin → control software
- C:\DBBC\doc → manuals
- C:\DBBC_CONF\                 → configuration text files
- C:\DBBC_CONF\FilesDBBC → firmware
Software

• General:

  *BASE Package*

  c:\DBBC\bin\DBBC client v3.exe (general client)
c:\DBBC\bin\clock1024.exe (CAT2 1024)
c:\DBBC\bin\clock2048.exe (CAT2 2048)
c:\DBBC\bin\ad9858.exe (CAT1)
c:\DBBC\bin\power.exe (on-off hardware)
c:\DBBC\bin\agc_if.exe (CoMo Unica3 test)
c:\DBBC\bin\agc_if_unica4.exe (CoMo Unica4 test)
Software on socket

- **DDC:**

  - `c:\DBBC\bin\DBBC2 Control DDC v104.exe` (server)
  
  - `c:\DBBC_conf\dbbc_config_file_104.txt`
  
  - `c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v104.bit`
  
  - `c:\DBBC\doc\DBBC2 DDC command set v104.pdf`
Example:

1  dbbc2_ddc_v101.bit  597.00  8  \(\rightarrow\) the first number is indication of ADB1\|2, in this case ADB1 is on
1  dbbc2_ddc_v101.bit  597.00  8  IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v101.bit  597.00  8  If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v101.bit  597.00  8  The second parameter is the firmware file name to be used.
2 dbbc2_ddc_v101.bit  597.00  8  The third and fourth parameters are frequency and bandwidth respectively.
2 dbbc2_ddc_v101.bit  597.00  8  Each Core2 board supports 4 bbcso if not present 0 has to be inserted in four lines
2 dbbc2_ddc_v101.bit  597.00  8
1 dbbc2_ddc_v101.bit  597.00  8
1 dbbc2_ddc_v101.bit  597.00  8
1 dbbc2_ddc_v101.bit  597.00  8
0 dbbc2_ddc_v101.bit  597.00  8
0 dbbc2_ddc_v101.bit  597.00  8
0 dbbc2_ddc_v101.bit  597.00  8

1 fila10g_v2_1.bit  \(\rightarrow\) if a FILA10G is installed set first version 1 (with ACE), second version (without ACE 2), otherwise 0
1 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 38000  \(\rightarrow\) no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH

107 112 0 0  \(\rightarrow\) phase calibration values
CAT2 1024  \(\rightarrow\) CAT1\|2 and sampling frequency
DDC: running **DBBC2 Control DDC v104.exe**

![Image of command output]

after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe** or **Field System**

DDC Mode Commands and Form Table (see documents)
**DDC settings and optimization**

- Phase optimization: to be performed with a synthesizer and the dedicated command at the system installation. To be repeated after a hardware modification in the stack or transportation. Periodically as a general check.

- Amplitude optimization: to be performed using phase cal tones injected in the receiver and ‘bpcal’ software from Haystack. To be repeated after a hardware modification, new receivers, etc. Periodically as a general check.

- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check.
Software on socket

- PFB:

  c:\DBBC\bin\ DBBC2 Control PFB v15.exe  (server)

  c:\DBBC_conf\ dbbc_poly_config_file_15.txt

  c:\DBBC_conf\FilesDBBC\ dbbc2_pfb_v15.bit

  c:\DBBC\doc\ DBBC2 PFB command set v15.pdf
Example:

10 dbbc2_pfb_12.bit ➞ the first number is indication of ADB1|2, in this case ADB1 is on IFa
21 dbbc2_pfb_12.bit and ADB2 on IFB, etc. The second number is the Core2 board address.
12 dbbc2_pfb_12.bit If no Core2 is inserted in the first and second column put 99.
13 dbbc2_pfb_12.bit Third parameter is the firmware file name to be used.
99 ACE.bit ➞ do not modify here
99 fila10g.bit ➞ if a FILA10G with ACE is installed in the DBBC JTAG chain set 01,
                 if a FILA10G without ACE is installed set 02, otherwise 99
1 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 58000 ➞ no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0 ➞ phase calibration values
CAT1 1024 ➞ CAT1|2 and sampling frequency
PFB: running **DBBC2 Control PFB v15.exe**

after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe or Field System**

PFB Mode Commands, Form Table , PFB Frequencies (see documents)
PFB settings and optimization

• Phase optimization: to be performed with a synthesizer and the dedicated command at the system installation. Values could be different by the DDC ones. To be repeated after a hardware modification in the stack or transportation. Periodically as a general check.

• Amplitude optimization: to be performed using phase cal tones injected in the receiver and ‘bpcal’ software from Haystack. To be repeated after a hardware modification, new receivers, etc. Periodically as a general check.

• Zero baseline with a second system if available, or intra-system at the installation and as a periodic check.
DSC
Software on socket

• Implemented inside PFB software and firmware with ‘dbbcmode=full’, so again:

  c:\DBBC\bin\DBBC2 Control PFB v15.exe (server)
  c:\DBBC_conf\dbbc_poly_config_file_15.txt
  c:\DBBC_conf\FilesDBBC\dbbc2_pfb_v15.bit
  c:\DBBC\doc\DBBC2 PFB command set v15.pdf
DSC settings and optimization

- Phase optimization: PFB recommendations
- Amplitude optimization: PFB recommendations
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check
- Dedicated test software developed and running on MK5B+
SPECTRA
Software on socket

• SPECTRA:

c:\DBBC\bin\ DBBC2 Control SPC v1.exe (server)

c:\DBBC_conf\ dbbc_spc_config_file_1.txt

  c:\DBBC_conf\FilesDBBC\ dbbc2_spc_v1.bit

  c:\DBBC\doc\ DBBC2 SPC command set v1.pdf
Example:
10 dbbc2_pfb_12.bit <- the first number is indication of ADB1|2, in this case ADB1 is on IFa
21 dbbc2_pfb_12.bit and ADB2 on IFB, etc. The second number is the Core2 board address.
12 dbbc2_pfb_12.bit If no Core2 is inserted in the first and second column put 99.
13 dbbc2_pfb_12.bit Third parameter is the firmware file name to be used.
99 ACE.bit <- do not modify here
99 fila10g.bit <- if a FILA10G with ACE is installed in the DBBC JTAG chain set 01,
                   if a FILA10G without ACE is installed set 02, otherwise 99
1 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 58000 <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0 <- phase calibration values
CAT1 1024 <- CAT1|2 and sampling frequency
Noto L band cal tones off
Noto L band cal tones on
How to set the FILA10G

• Download the firmware is automatically made by the DDC/PFB control software
• In the FILA-SA a script file can be used with the additional included Xilinx Jtag programmer
• Communication is through serial port or Ethernet in the stand-alone version
• Commands available (see document)
• VDIF packet size setting (see document)
• Script files can be used for block of commands (see batch)
• FILA10G Files:

  c:\DBBC\bin\timesyncFILA10G.exe (MK5B time set)

  c:\DBBC\bin\vdif_timesyncFILA10G.exe (VDIF time set)

  c:\DBBC\bin\sendstr.exe (serial communication)

  c:\DBBC_conf\FilesDBBC\fila10g_v2.bit

  c:\DBBC\doc\DBBC2 FILA10G Command set v2.pdf

  Note: a program to sync with a NTP server is required
  (ex. NetTimeSetup-314.exe)
Commands integrated in DDC v105 (under way) and PFB v15

\texttt{fila10g = synch, [YYYY-MM-DD: hh:mm:ss]}

Synchronize the FILA10G clock.
Arbitrary time optionally set.

\texttt{fila10g = time}
Reports FILA10G time and difference with respect to DBBC-PC time in seconds.

\texttt{fila10g = mode, format, source, packetsize}

format => 5b | vdif
source => vsi1 | vsi2 | vsi1-2 |
\hspace{0.1cm}vsi1 and vsi2 are 2 Gbps modes, vsi1-2 is 4 Gbps mode
\hspace{0.1cm}| test-2-0 | test-2-1 | test-2-b | test-2-t | test-4-0 | test-4-1 | test-4-b | test-4-t |
\hspace{0.1cm}‘test-2-x’ are 2Gbps modes, ‘test-4-x’ are 4Gbps modes
packetsize => data frame size in single thread mode: 64,80,128,160,200,256,320,400,512,640,800,1000,1024,1280,1600,2000,2048,2560,3200,4000,4096,5000,5120,6400,8000,8192
\hspace{0.1cm}on both eth0 and eth1 ports.

\texttt{fila10g = start | stop}
Run or stop the 10G packets on both eth0 and eth1 ports

\texttt{fila10g = cmd = direct command}
direct command is sent as recognized by the FILA10G.
DBBC3 - Full digital VLBI2010
DBBC3

• Project supported by EU Radionet3
• Partners:
  INAF – Italy
  MPIfR - Germany
  OSO – Sweden
• Starting date July 2012, duration 3 years
Twofold implementation

• Astronomic VLBI: 32Gbps EVN, mmVLBI

• Geodetic VLBI: VLBI2010
DBBC3 General Performance for EVN

- Number of Input IF: 1 - 4
- Instantaneous bandwidth ea. RF: \(\geq 4\) GHz
- Sampling representation: 10 bit
- Processing capability: \(\text{max } 10\) TMACS (multiplication-accumulation per second)
- Output: VDIF Ethernet packets, \(\geq 32\) Gbps
- Compatibility with existing DBBC environment
DBBC3 General Performance for VLBI2010

• Number of Input IF: 1 - 4
• Instantaneous bandwidth ea. RF: =14-16 GHz
• Sampling representation: 8 bit
• Processing capability: max 10 TMACS (multiplication-accumulation per second)
• Output: VDIF Ethernet packets, >=64Gbps
• Compatibility with existing DBBC environment
Typical DBBC3 Architecture for EVN

- ADB3-L
  - 10 bit Sampler
  - Synthesizer

- CORE3-L
  - DDC PFB DSC
  - Management

- FILA40G
  - PACKETS HANDLING
  - BUFFER
  - 40G
  - Management

Connections:
- Receiver IF Left/Right
- 2 x 4 GHz bwd

Networks:
- 4 x 10 GE
- 1 x 40 GE

Storage:
- Disk Storage

Network to buffer cloud / correlator

40/100G network to buffer cloud / correlator
Typical DBBC3 Architecture for VLBI2010

DBBR - Digital Broad Band VLBI2010 Receiver

8 bit Sampler → DDC PFB DSC

Receiver IF
Left/Right
2 x 14 GHz bwd

Synthesizer → Management

ADB3-H

CORE3-H

1 x 40 GE

10/40/100G network to buffer cloud / correlator

FILA40G

PACKETS HANDLING

BUFFER

40G

Management

Disk Storage

DBBC2010 performs this functionality

8 x 1 GHz bwd

4 x 10 GE

ADC3-H adapter

Synthesizer

ADB3-H adapter

DDC PFB DSC

Management

Receiver Digital IF Left/Right

Receiver IF Left/Right

8 x 1 GHz bwd
DBBR – Digital Broad Band Receiver

- Fully digital receiver at sky frequency
- Feed developed in Italy
- Feed and LNA at cryogenic temperature
- Sky frequency sampling
- Digital down conversion
- Output based on Digital Optical Link
DBBR

Dual Pol Ridged Feed

Cryogenic Dewar Wideband (2-14 GHz) LNAs

ADB3-H & Core3-H Set of shielded boxes

Wideband (2-14 GHz) Amplifier Chain

Cable with 16 Optical Fibers
to ADB3-H adapter
ADB3-H General Performance

- **ADB3-H:**
  - Number of IFs: **4**
  - Equivalent Sample Rate ea. IF: **28.672 GSps**
  - Instantaneous bandwidth ea. IF: **14.336 GHz**
  - Sampling representation: **8 bit**

- Real Sampling
- Compatibility with existing DBBC environment
- **Engineers samples available, commercial devices expected in fall 2013**
ADB3-H Sampler

10 MHz → Sampling Clock Generation

1 PPS →

14 GHz → Sampler 1 → Serial Link TX

24 x 11.2 Gbps

14 GHz → Sampler 2 → Serial Link TX

24 x 11.2 Gbps

14 GHz → Sampler 3 → Serial Link TX

24 x 11.2 Gbps

14 GHz → Sampler 4 → Serial Link TX

24 x 11.2 Gbps

24 x 11.2 Gbps
CORE3-H General Performance

- **Core3-H**
- Number of Input: max 48 serial links 11.2Gbps
- Number of Output: max 48 serial links 11.2Gbps
- Input Sampling Representation: 8-10 bit
- Processing capability: max 5 TMACS (multiplication-accumulation per second)
- Processing capability: WB-DDC, WB-PFB, DCS
- Output: VDIF Ethernet packets, >=32Gbps
- Compatibility with existing DBBC environment
- **DDC Firmware under development on prototype board**
CORE3-H

Max
48 x 11.2Gbps

Serial Link RX

HSI

Processing Unit 3 TMACS

HSO

Serial Link TX

Max
48 x 11.2Gbps
8 x 12.5Gbps

8 x 12.5Gbps

Pass-band

-100 dB
ADB3-L General Performance

- **ADB3-L:**
  - Number of IFs: 2
  - Equivalent Sample Rate ea. IF: 8 GSps
  - Instantaneous bandwidth ea. IF: 4 GHz
  - Sampling representation: 10 bit
- Real/Complex Sampling
- Compatibility with existing DBBC environment
- **First prototype successfully tested, pcb project of the module ready**
ADB3-L Sampler

10 MHz
1PPS

Sampling Clock Generation

1 x 4 GHz

Sampler 1

1 x 4 GHz

Sampler 2

4 x 1 GHz

ADB3-H Adapter

8 x 10Gbps
8 x 10Gbps

Serial Link TX
CORE3-L General Performance

- Core3-L
  - Number of Input: max 16 serial links 10Gbps
  - Number of Output: max 16 serial links 10Gbps
  - Input Sampling Representation: 8-10 bit
  - Processing capability: max 3 TMACS
    (multiplication-accumulation per second)
  - Processing capability: WB*-DDC, WB*-PFB, DCS
  - Output: VDIF Ethernet packets, >=32Gbps
  - Compatibility with existing DBBC environment

- Same device of Core3-H in reduced pin-out version
- DDC and PFB Firmware to be derived from the current DBBC2

* Wide band
CORE3-L

- 16 x 10Gbps
- 4 x 12.5Gbps

Max

Serial Link RX

HSI

PROCESSING UNIT
3 TMACS

HSO

Serial Link TX

Max

4 x 12.5Gbps

CCM
FILA40G Single Module General Performance

• Serial Link Input: = 4 x 10Gbps
• Serial Link Output: = 1 x 40Gbps
• Packets manipulating capability (filtering, pulsar gating, burst mode, etc.)
• Packets forwarding capability (different correlator nodes, different correlator sites, etc)
• Packets monitoring capability
• SAS ports for storage
• Project under definition
FILA40 Architecture

Single Module

- Large Area Buffer
- 40G Packet Forwarding Engine
- 40G 4 lambda transceiver
- User interaction and monitoring
- Packet Management
- Storage

Connections:
- 4 x 10 Gbps
- 1 x 40 Gbps
- GLASS

- 40G Packet Forwarding Engine
- 1 x 40 Gbps

- Packet Management
- 4 x 10 Gbps
**FILA 40G Single Module**

### Dual Xeon E5-2600

Software operations on data e.g.

- Pulsar gating
- Combine 4x 8 Gbps streams to 1x 32 Gbps

Final datastream sent via 40G NIC or written to disk array

Each SAS2 HBA provides min. 16 Gbps write speed to 32 + disks

SAS3 doubles per-port bandwidth

→ SAS3 HBAs should provide min. 32 Gbps write to 64+ disks