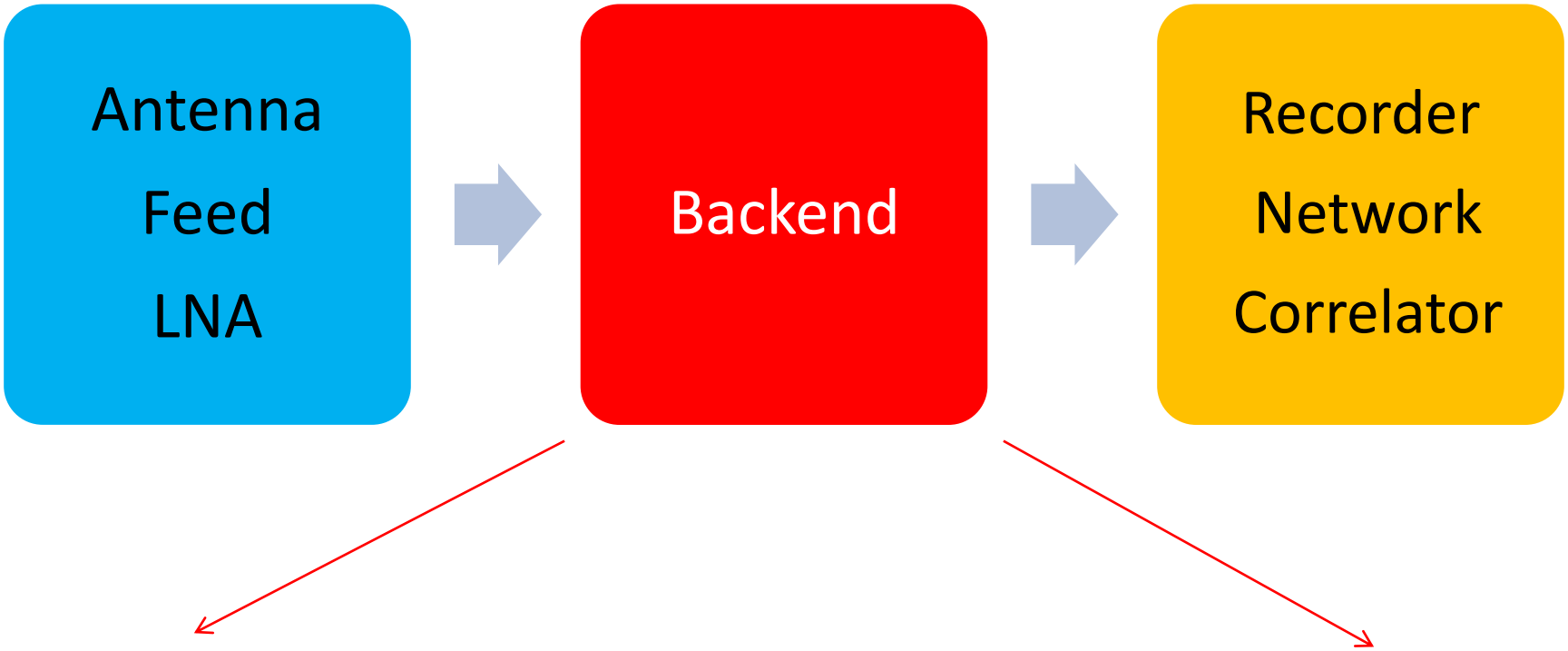
DBBC2 Setup and Operations

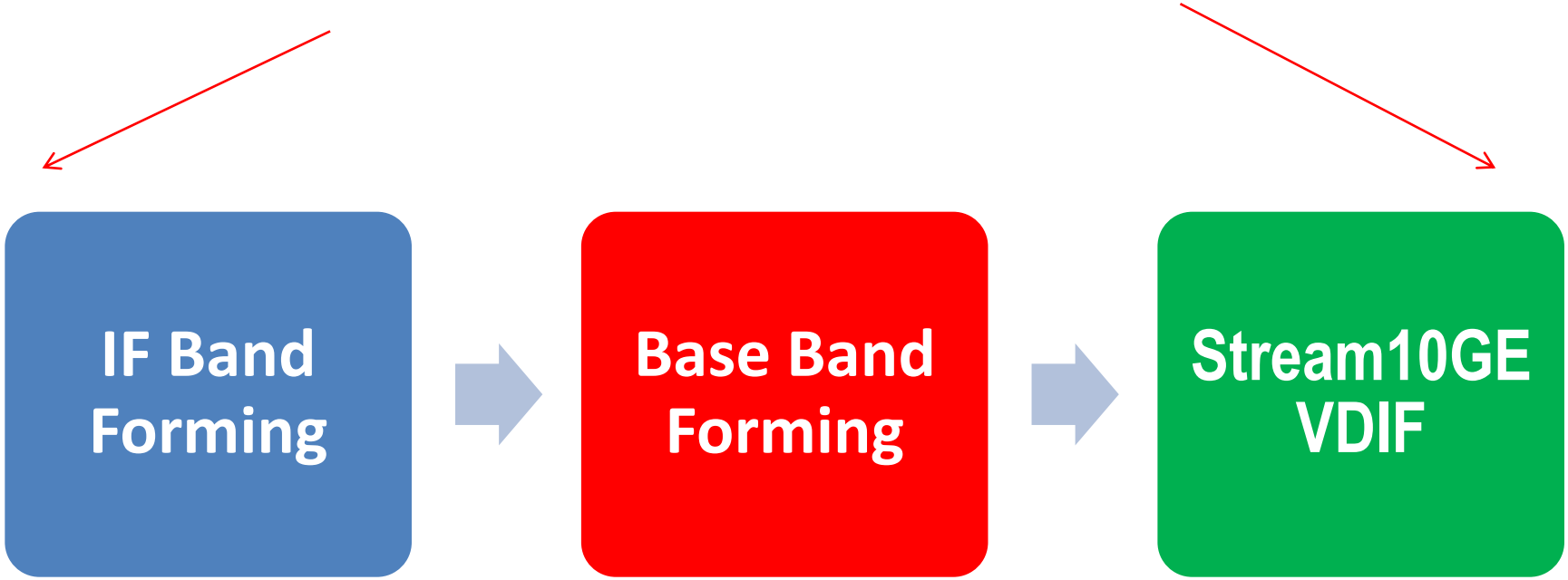
G. Tuccari

General Functionality



General Functionality

Backend Schematic Block

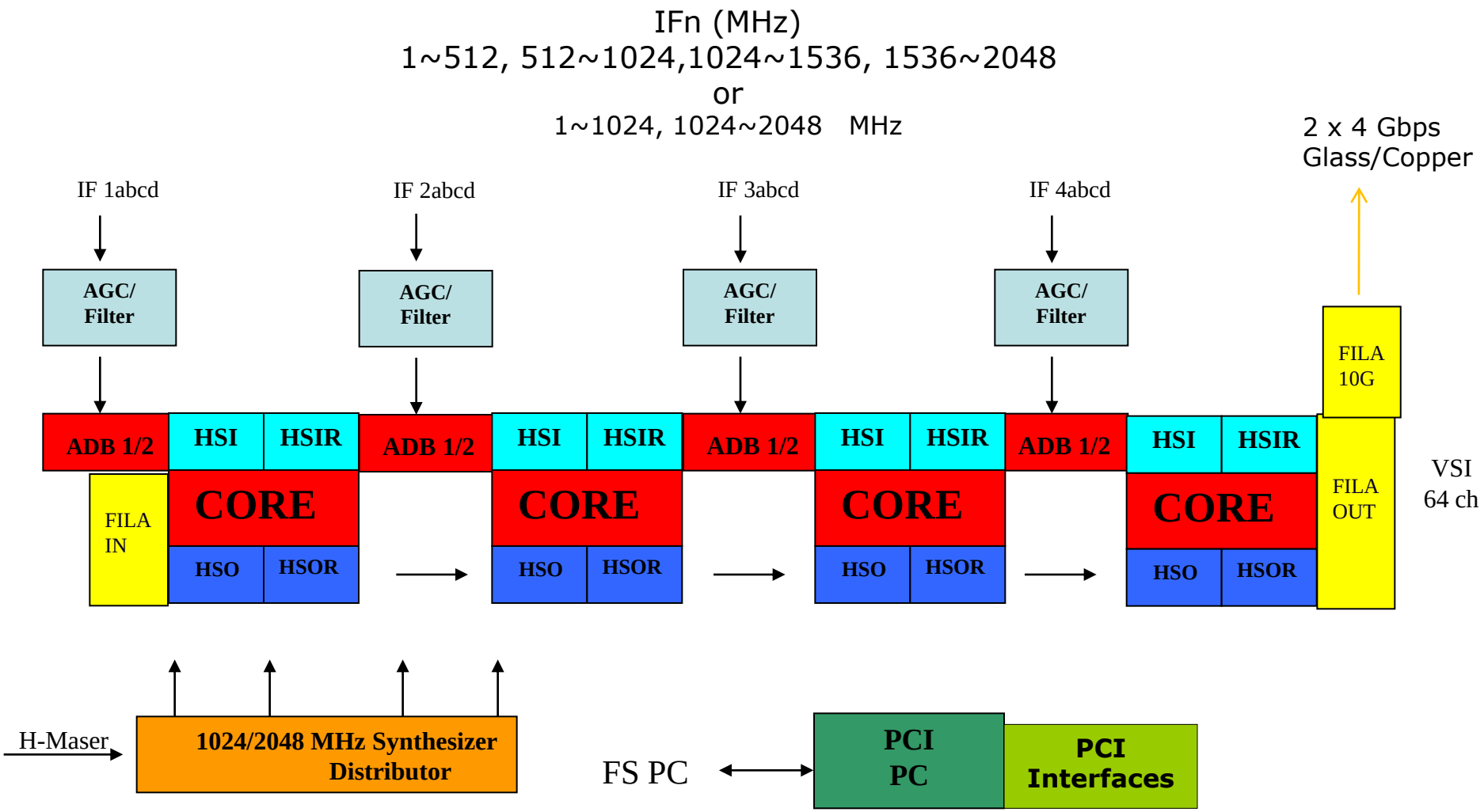


DBBC2 /DBBC2010 General Features

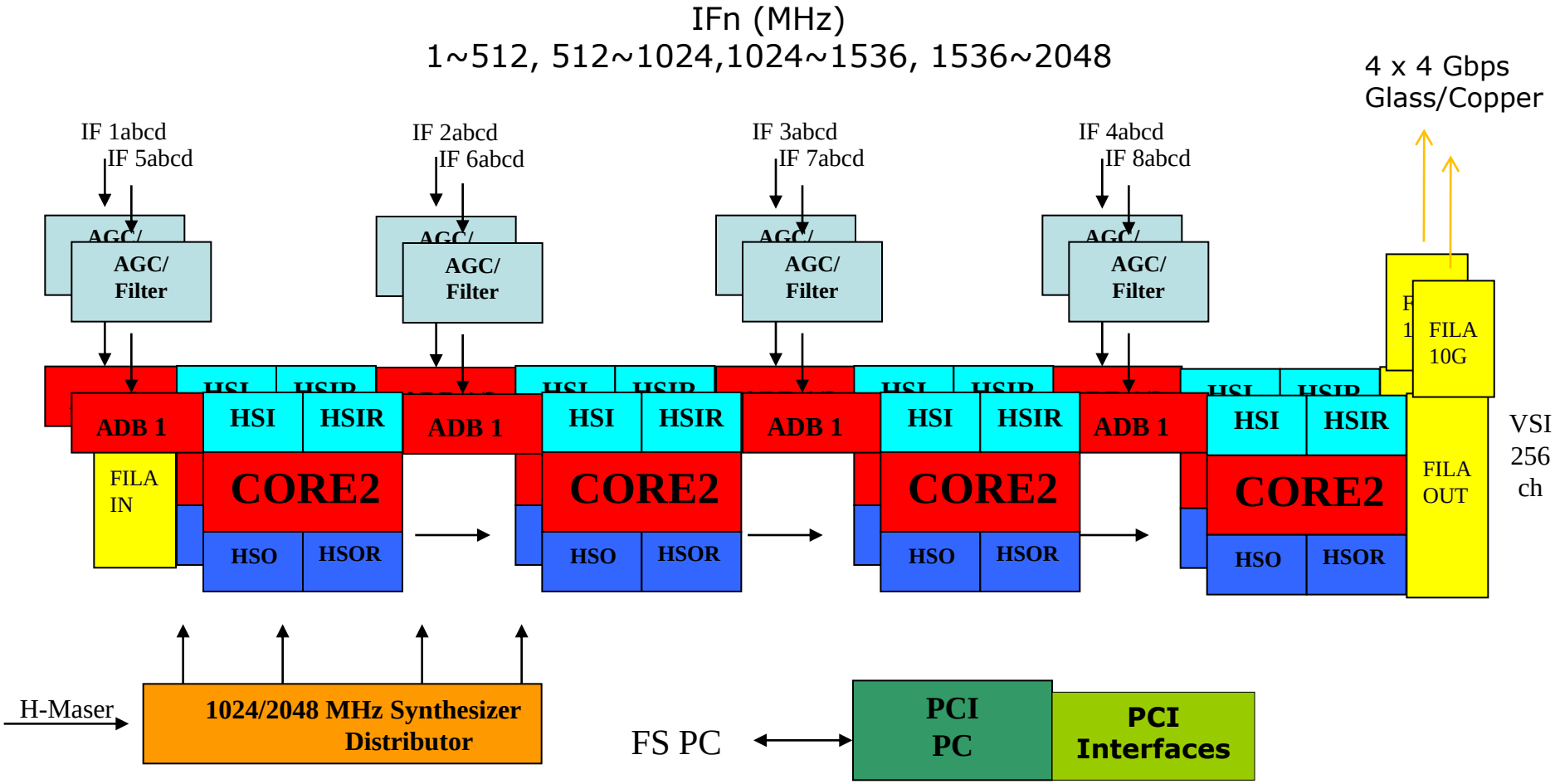
- 4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz
- 1024/2048 MHz sampling clock frequency
- More personalities for different observing modes
- Input 4/8 polarizations / bands
- Output 4/8 groups of 32 data channel
- Output as VSI interfaces or as 10G Ethernet streams
- Control under Field System or other client console

DBBC
Hardware Structure

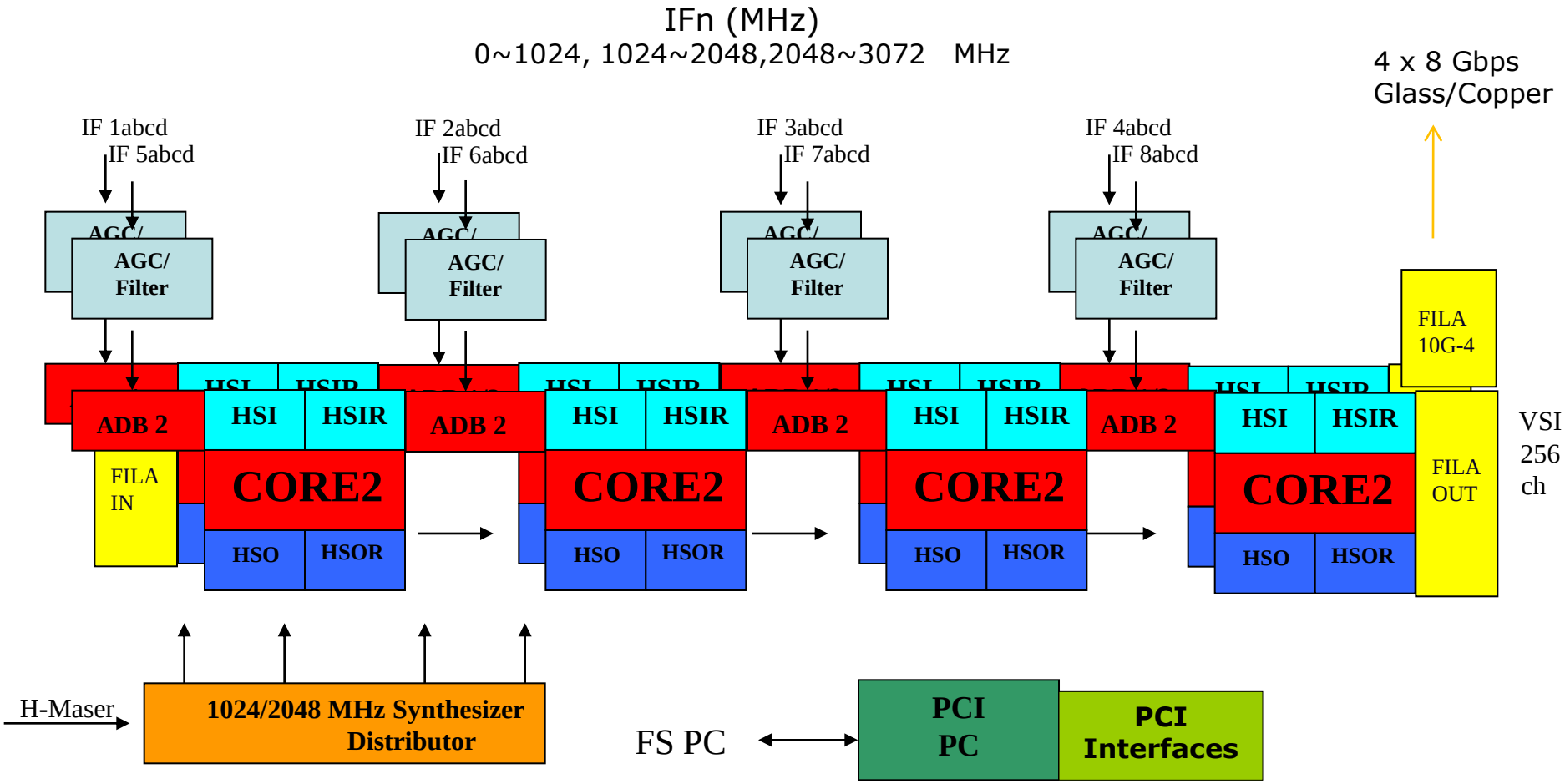
DBBC2 Architecture



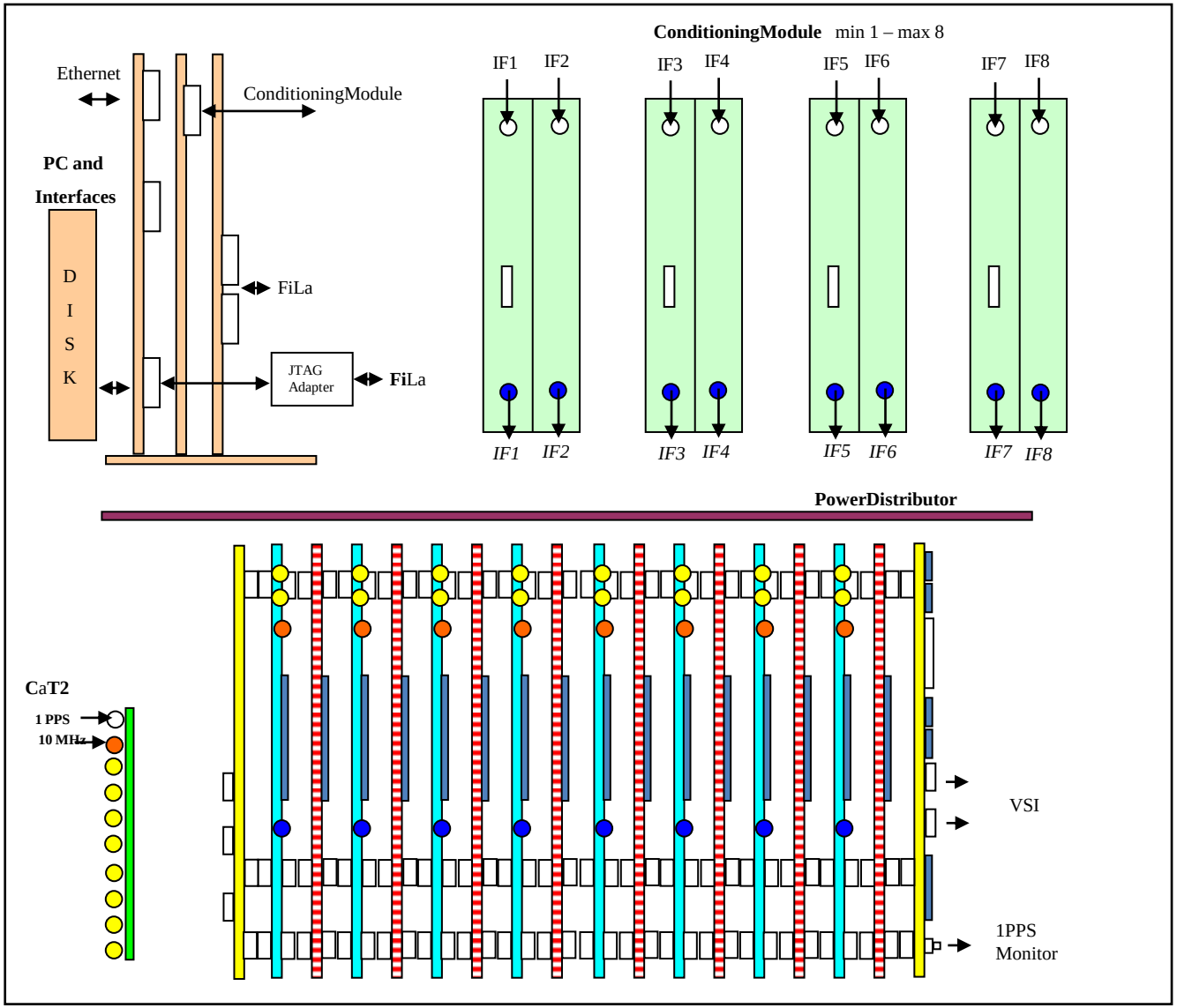
DBBC2010 - Half VLBI2010 Compliant
8 IFs @ 512 MHz
Output data rate 16 Gbps



DBBC2010 - Full VLBI2010 Compliant
8 IFs @ 1024 MHz
Output data rate 32 Gbps



DBBC2 / DCCB2010
Schematic Top View

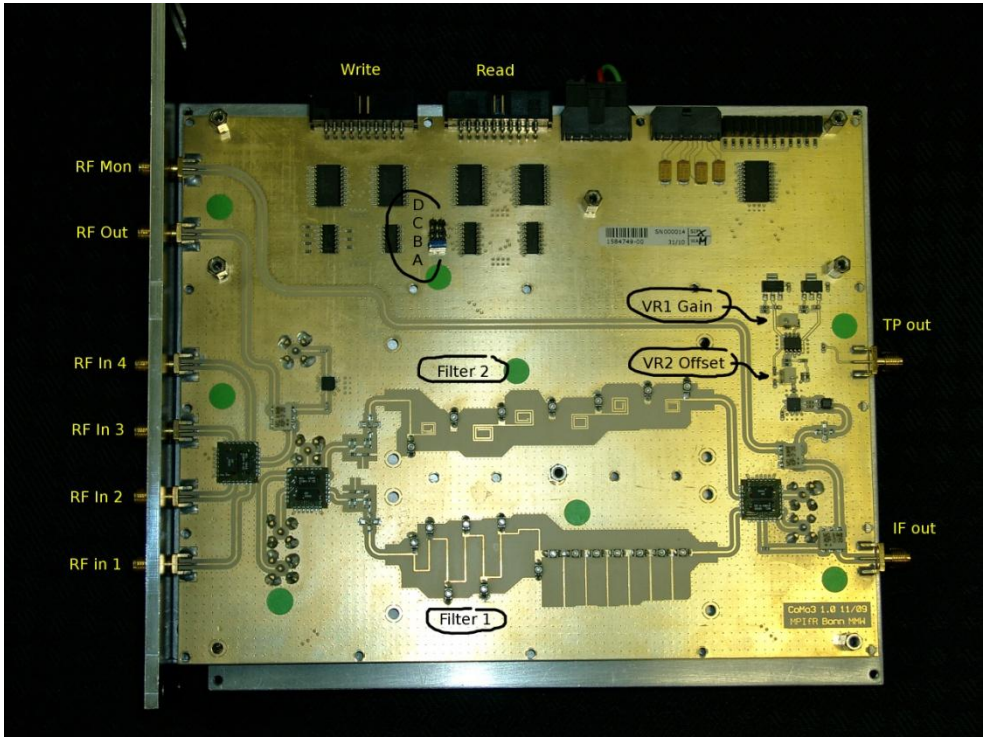


FiLa IN **STACK = ADB1/2 - Core2** (min 1 – max 8) **FiLa OUT**

Review of the System Components

- Analog Conditioning Module - CoMo
- Analog-Digital Converter (ADB1 - ADB2)
- Data Processing (Core2)
- Connection and Service
  (FiLaIN/OUT – FiLa10G FILA10G-4)
- Timing and Clock (CaT2 – Clock and Timing)
- Computer Control (PCSet)

Conditioning Module (Unica3)



4 selectable RF input

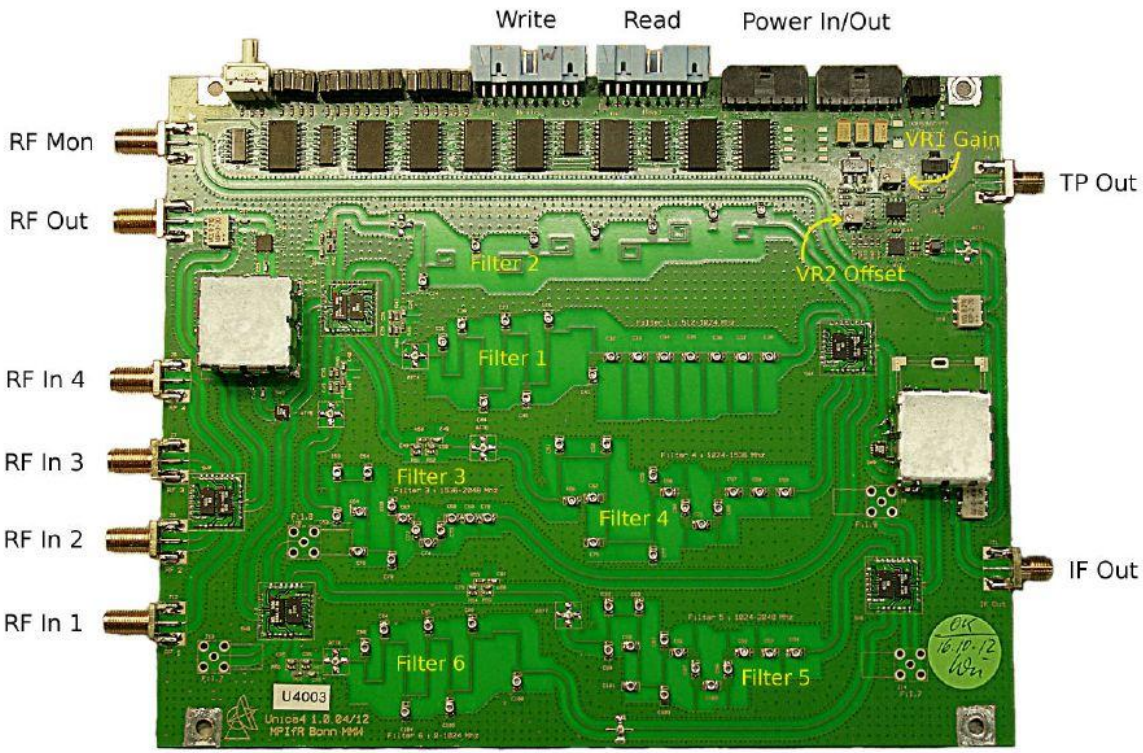
4 selectable Nyquist Filters

31.5 dB Programmable Attenuation

Total Power Full Band

Manual or Automatic Gain Control

Conditioning Module (Unica4)



4 selectable RF input

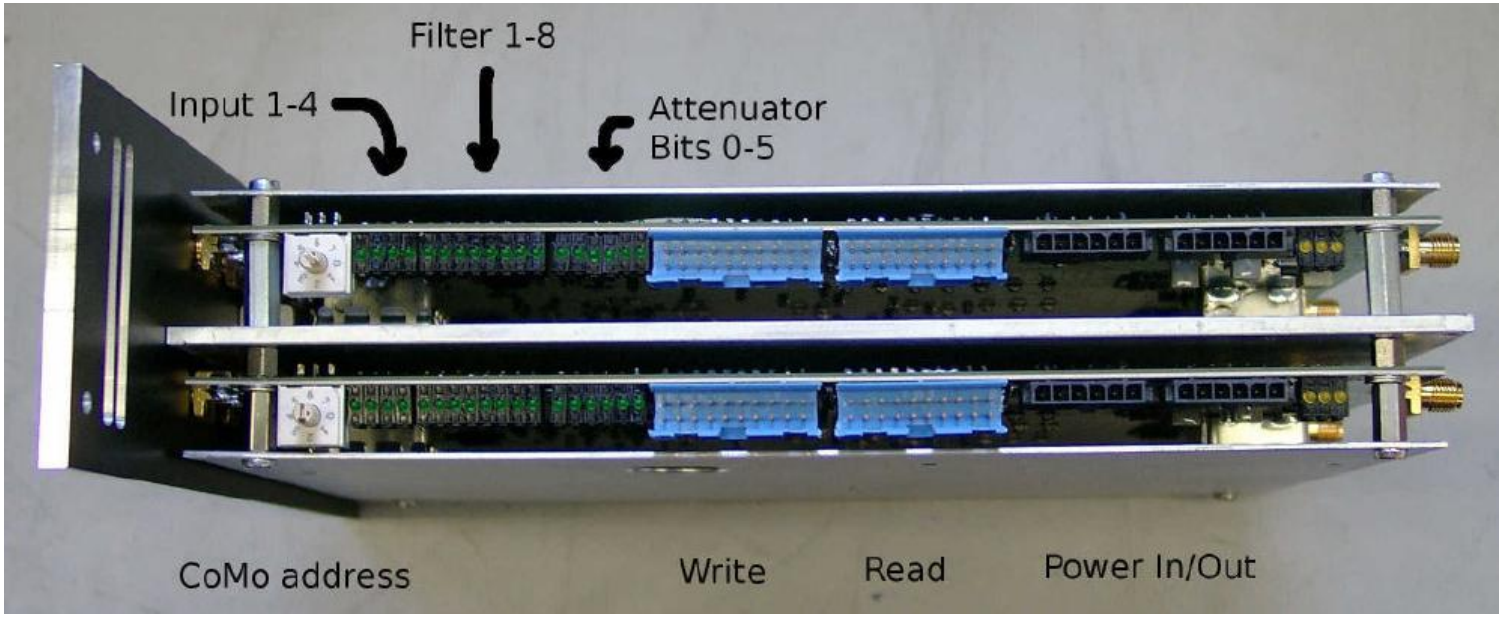
8 selectable Nyquist Filters

31.5 dB Programmable Attenuation

Total Power Full Band

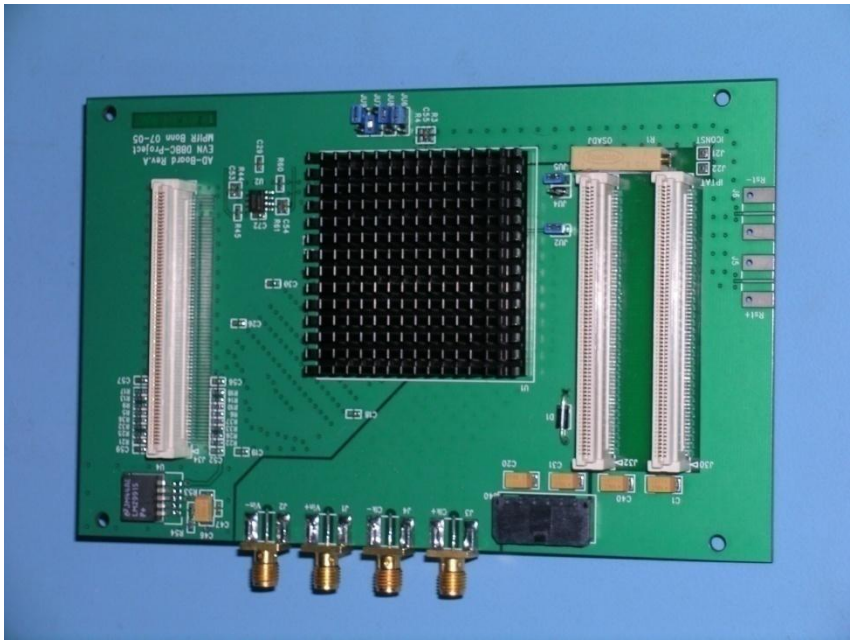
Manual or Automatic Gain Control

1 CoMo includes 2 Unica4



ADB1

Analog to Digital Converter



Analog input: 0 - 2.2 GHz

Max Sampling clock single board: 1.5 GHz

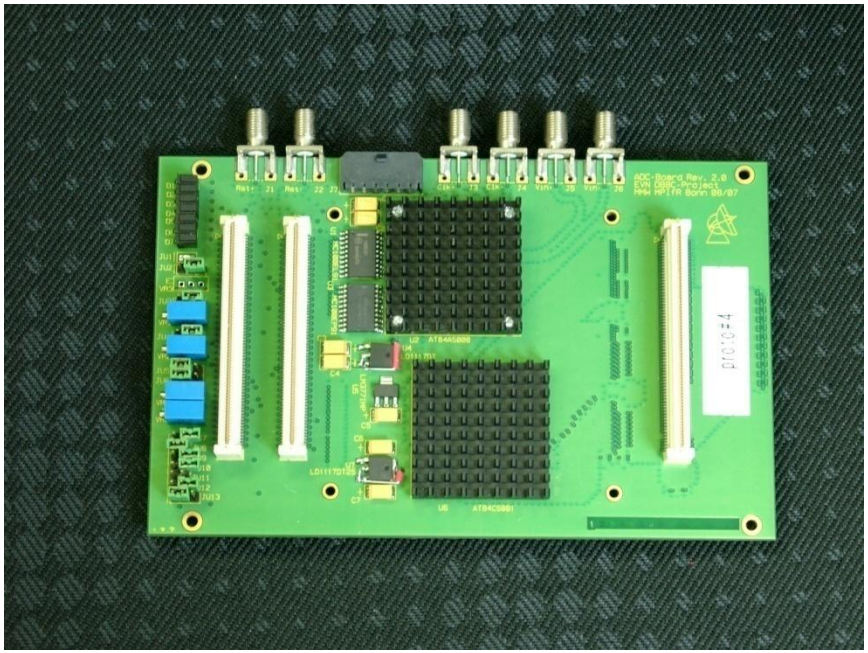
Max Istantaneous Bandwidth in Real Mode: 750 MHz

Max Istantaneous Bandwidth in Complex Mode: 1.5 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR

ADB2

Analog to Digital Converter



Analog input: 0 – 3.5 GHz

Max Sampling clock single board: 2.2 GHz

Max Istantaneous Bandwidth in Real Mode: 1.1 GHz

Max Istantaneous Bandwidth in Complex Mode: 2.2 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR
4 x 8-bit @ 1/8 SClk DDR

Piggy-back module support for 10-bit output and connection with FiLa10G board.

Core2

Basic processing unit

Input Rate:
(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s
(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s
More…

Typical Output Rate:
(64 ch x 32-64-128) Mb/s

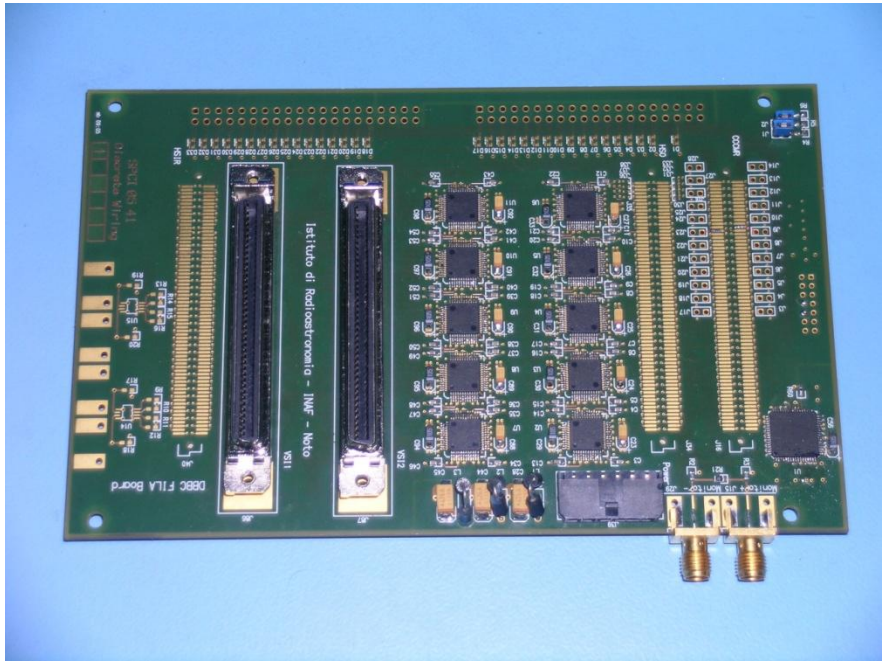
Programmable architecture

Es. Digital Down Converter:
1 Core2 = 4 BBC
1 Core2 = 1 Polyphase 16 Filter Bank

1 VSI 32 ch output in piggy-back

FiLa Board IN/OUT

Connection and Service



First and Last board in the stack

First:

- Communication Interface
- JTAG Programming Channel
- 1PPS Input

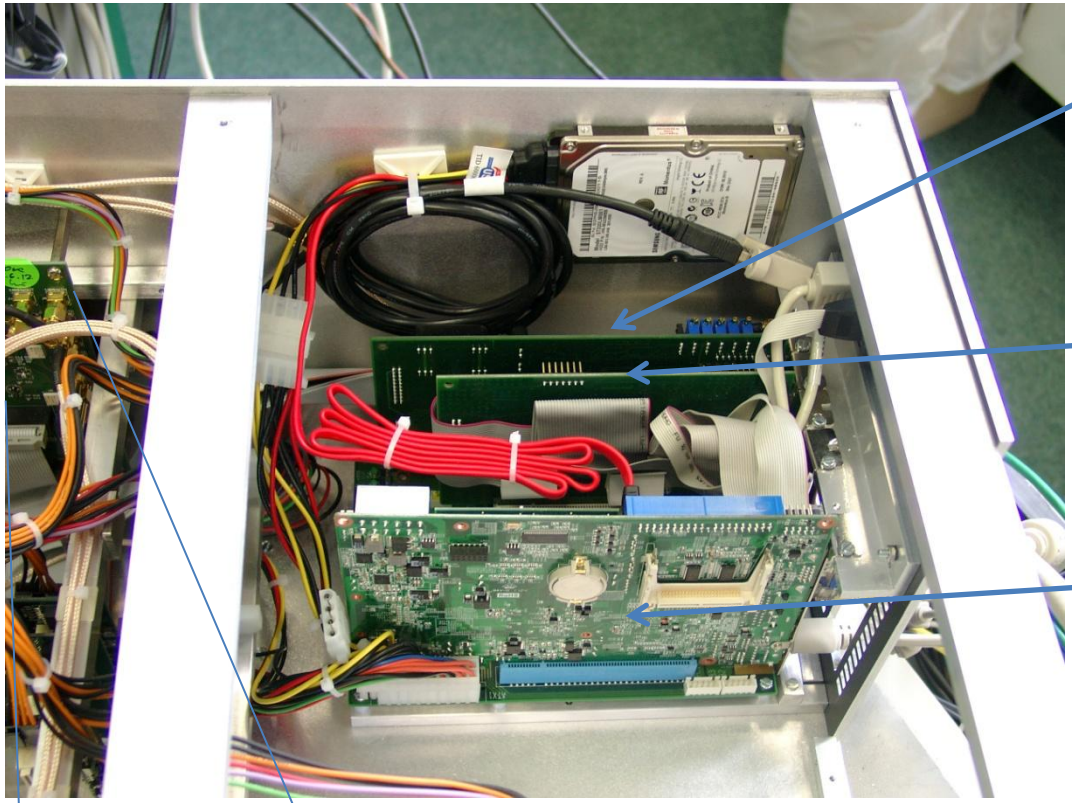
Last:

- 2 VSI Interfaces

1PPS Monitor Out

80Hz Continuous Cal Out

PCSet



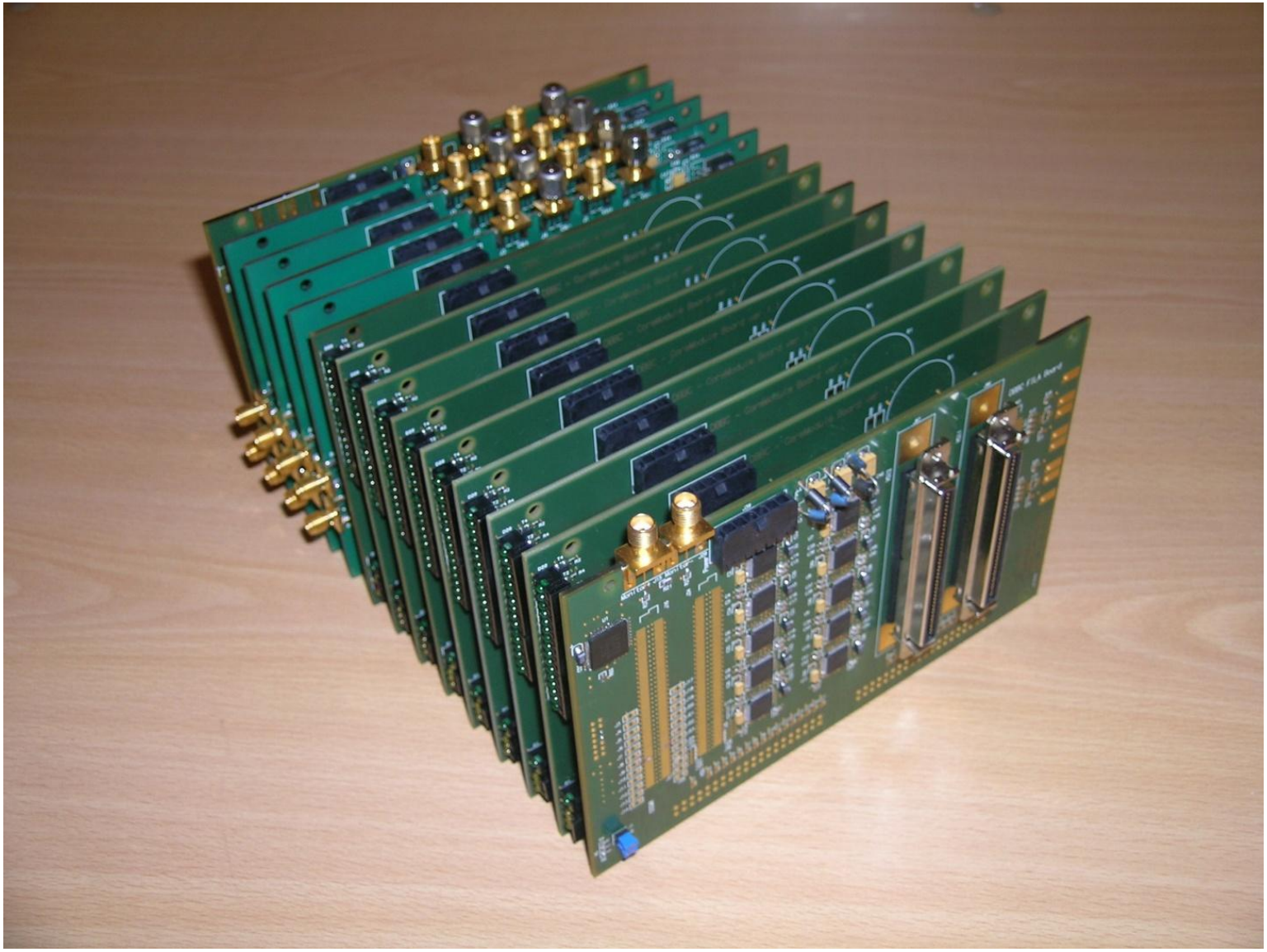
ADLink PCI9111HR:
Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control, etc.

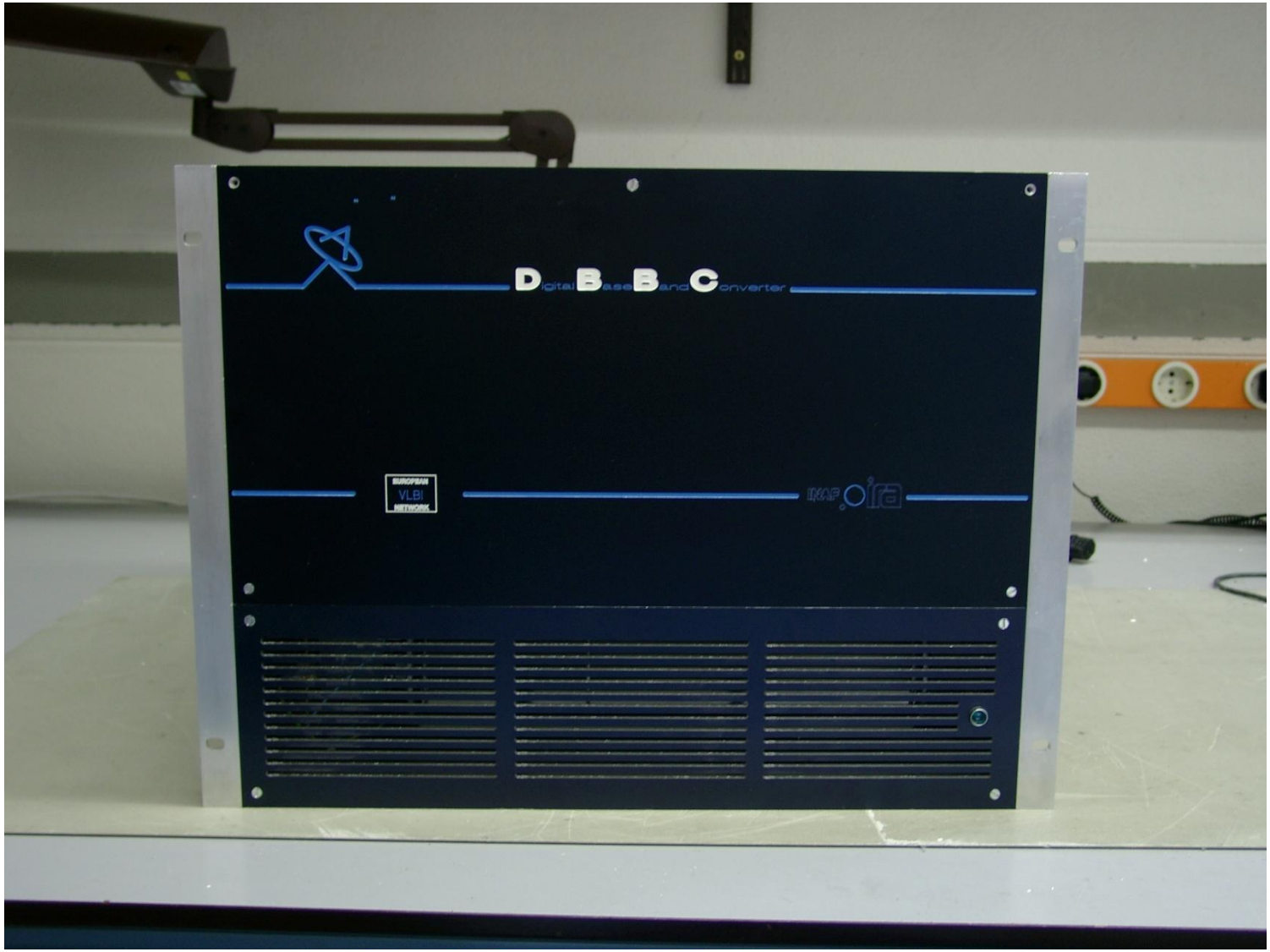
ADLink PCI7200:
Communication with 32-bit bus for Core2 register setting, total power measurement, state statistics, etc.

Adventech PCI-7030:
Half Size PCI Motherboard (Intel Atom) on PCI backplane

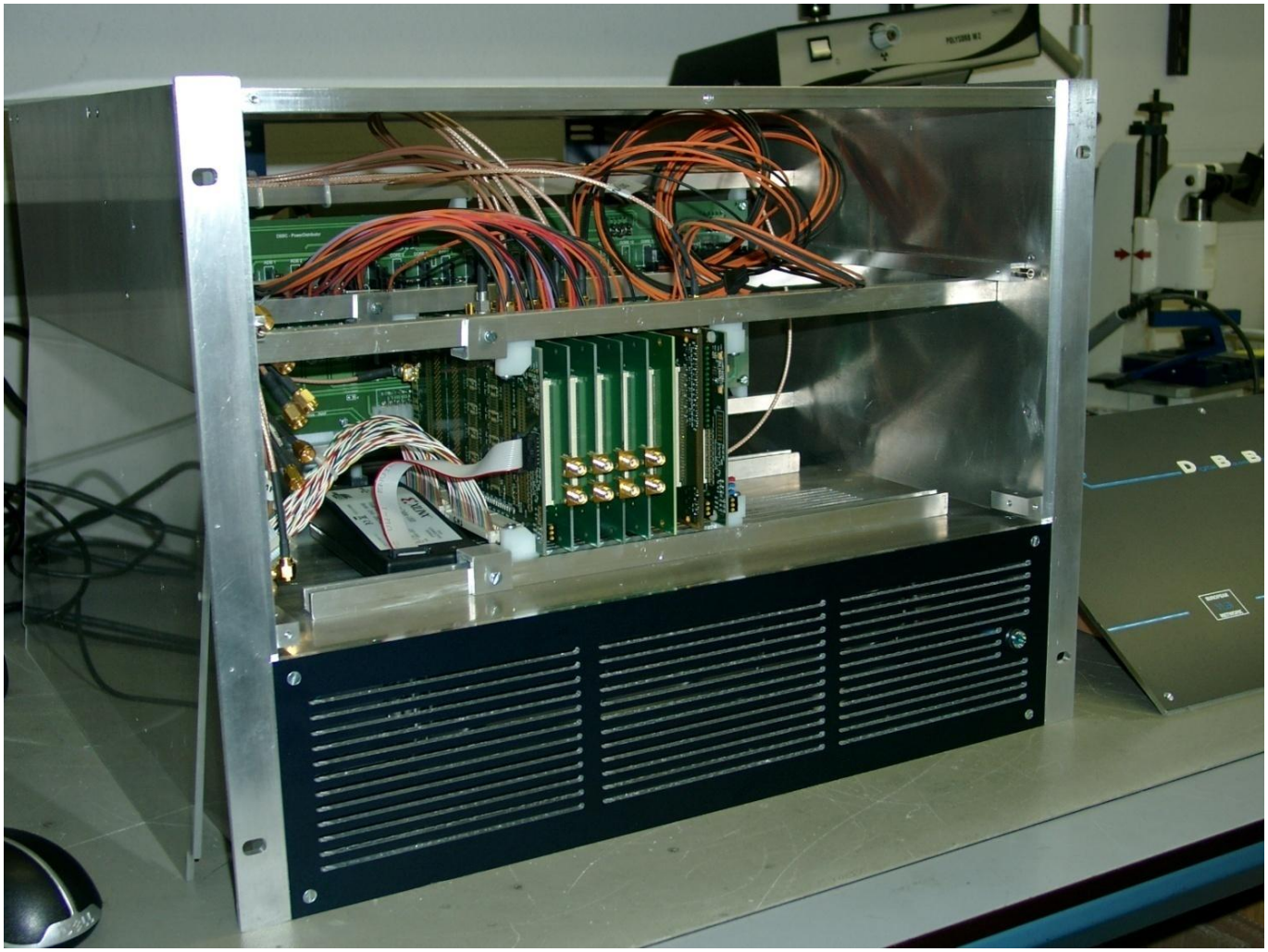
Xilinx programmer:
FPGA device configuration through USB – JTAG interface

DBBC2 Module Stack



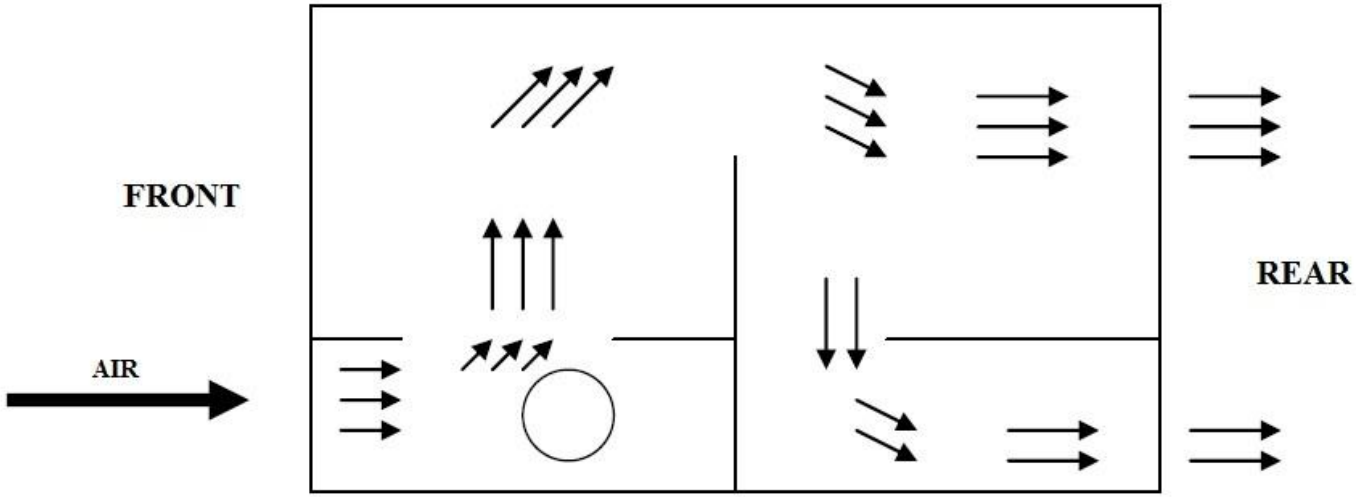

Digital Base Band Converter
EUROPEAN
VLBI
NETWORK
IRAF
ira


NI 2
ANALOG
TOT



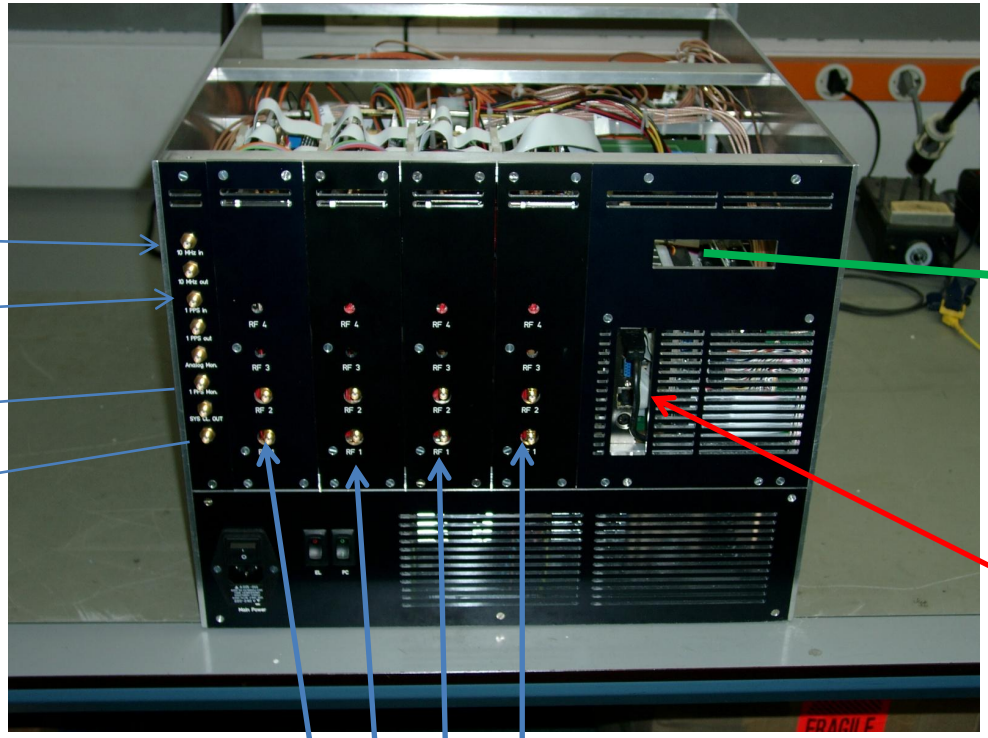

10 MHz In
10 MHz out
1 PPS In
1 PPS out
Analog Mon.
1 PPS Mon.
SYS LL OUT
RF 4
RF 3
RF 2
RF 1
Main Power
FRAGILE

DBBC Box: air-flow path



The air cooling flow from a side view

How the DBBC is to be connected in your control room



10 MHz

H-Maser
1PPS

1PPS test out

80 Hz cont cal

VSI-H

monitor
keyboard
mouse
network

RF/IF input

FiLa10G

10G Optical Fiber Ethernet Board

- Triangle connection between HSI (DBBC fast sampled data bus) – VSI – 10Gb link
- It can be placed either at the beginning or at the end of the stack chain → 10G link / MK5C
- Piggy-back board for ADB2

FILA10G main features

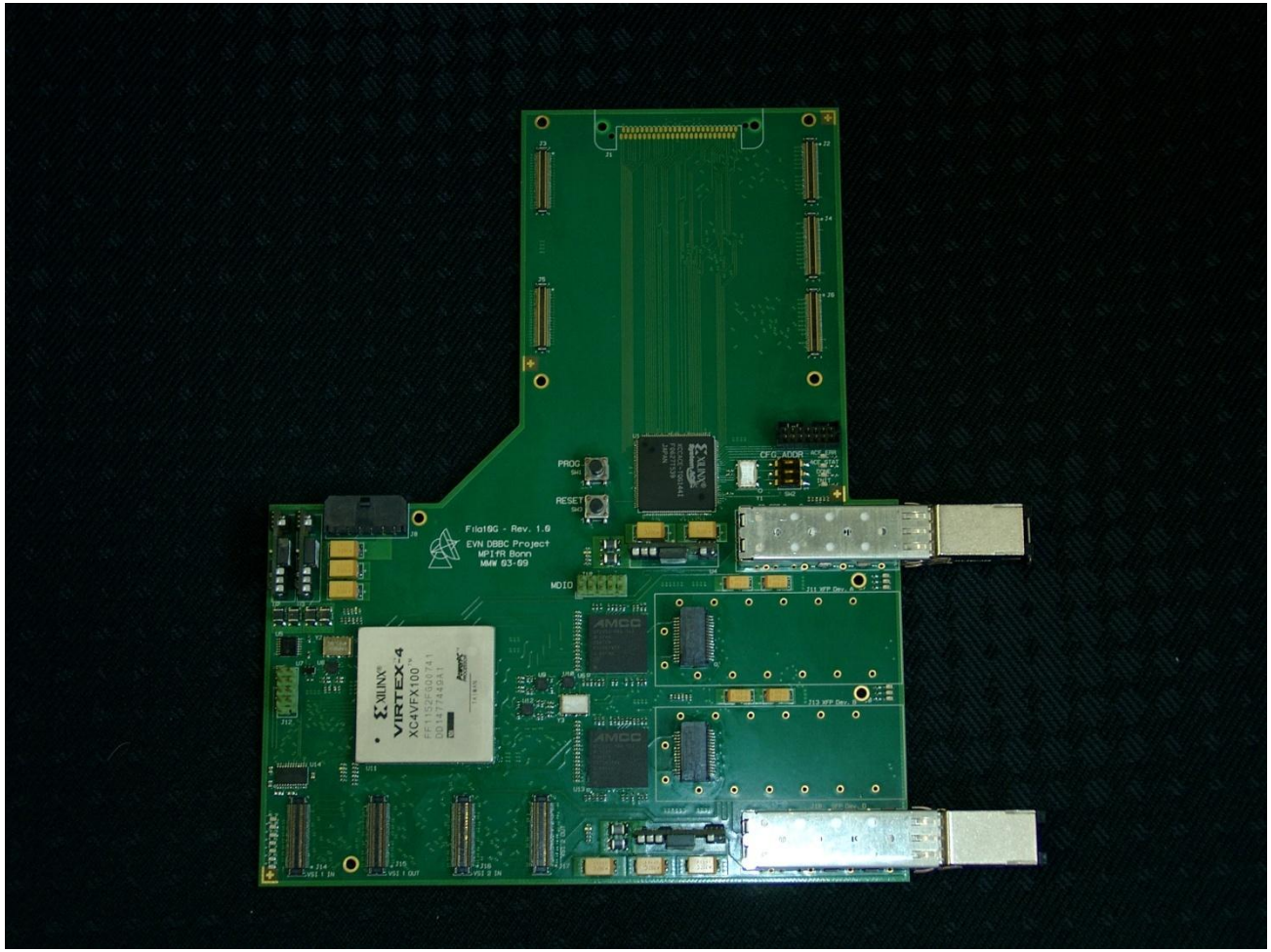
- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 Gbps each 10G port
- Format mode: MK5B in two 5008 bytes packets

  VDIF-ST in any allowed packet size

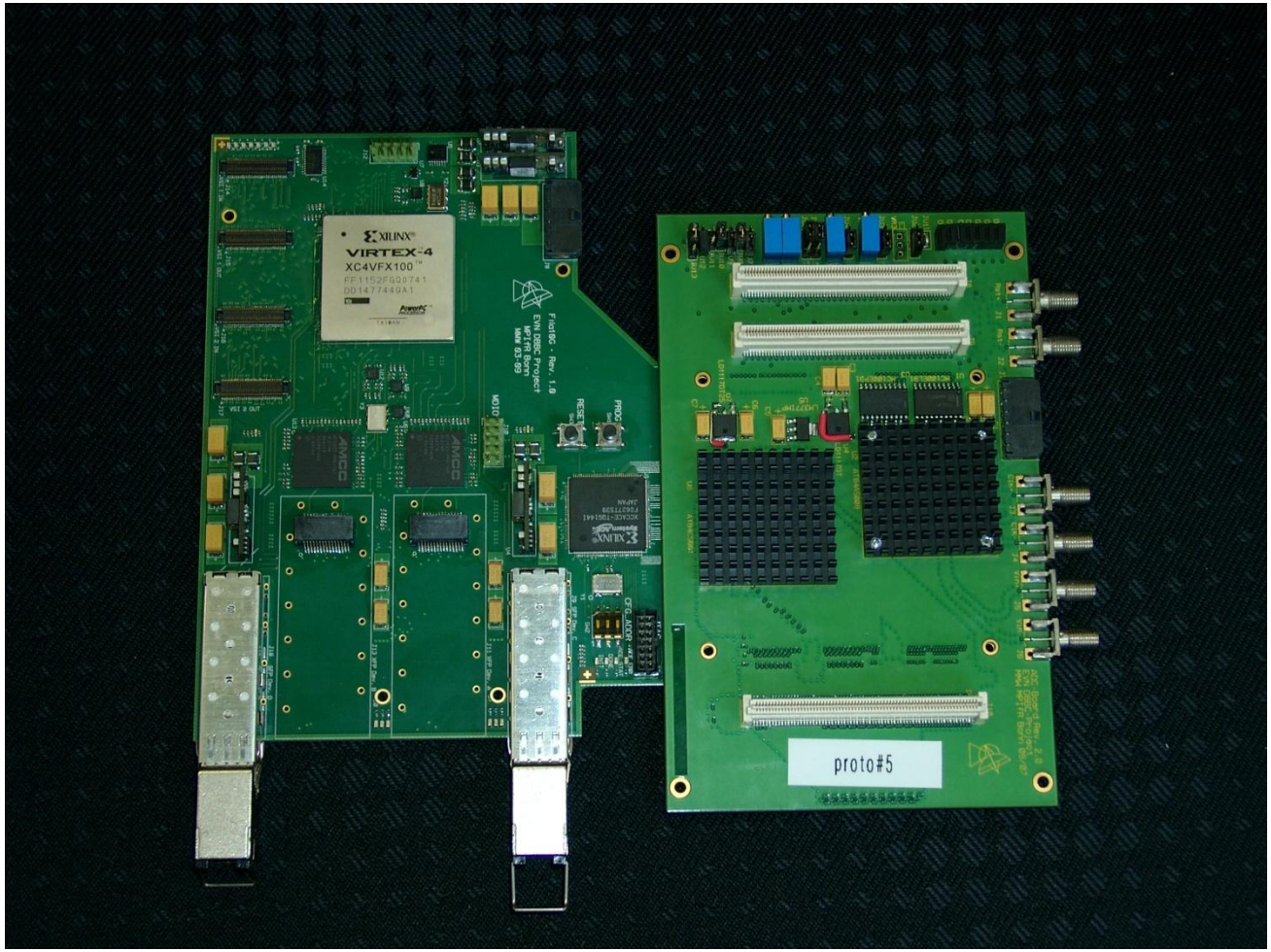
  VDIF-MT corner turned under development

  in any allowed packet size

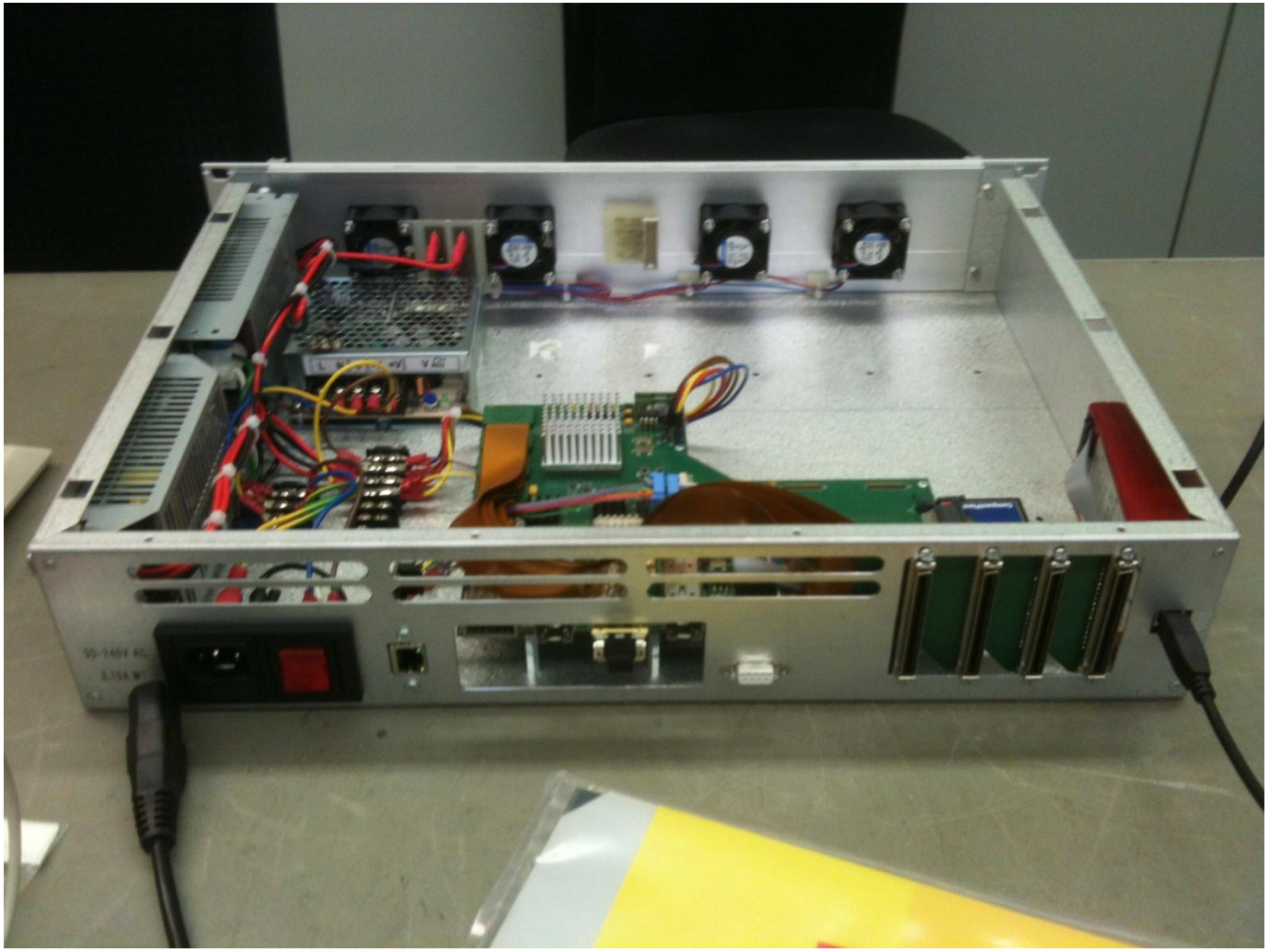
FILA10G


PROG
RESET
CFG_ADDR
Fila10G - Rev. 1.0
EVN DBBC Project
MPIfR Bonn
MAW 03-09
MDIO
XILINX
VIRTEX-4
XC4VFX100
AMCC
AMCC

FILA10G and ADB2

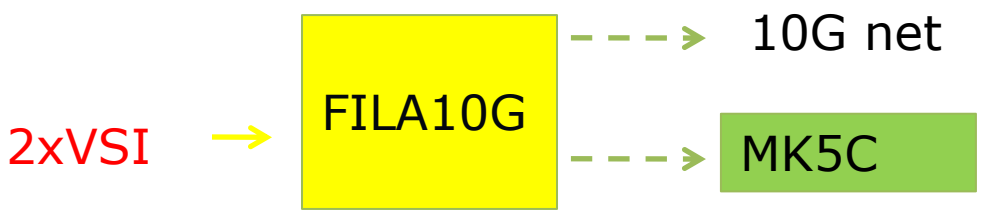


FILA10G - SA

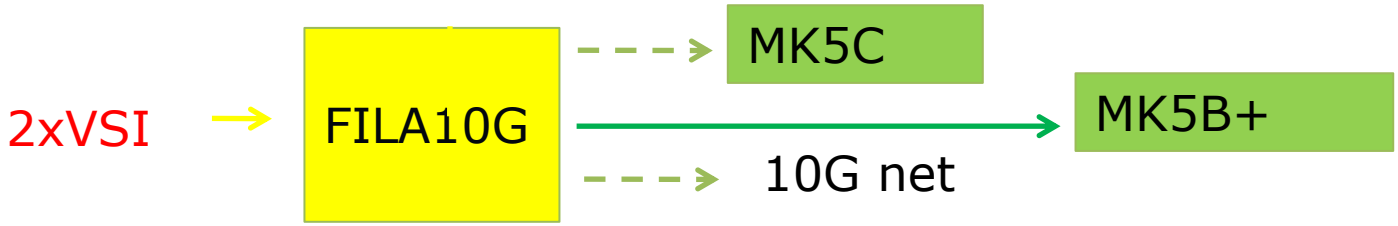


Connection examples

- 2 x VSI --> MK5C & 10GE net

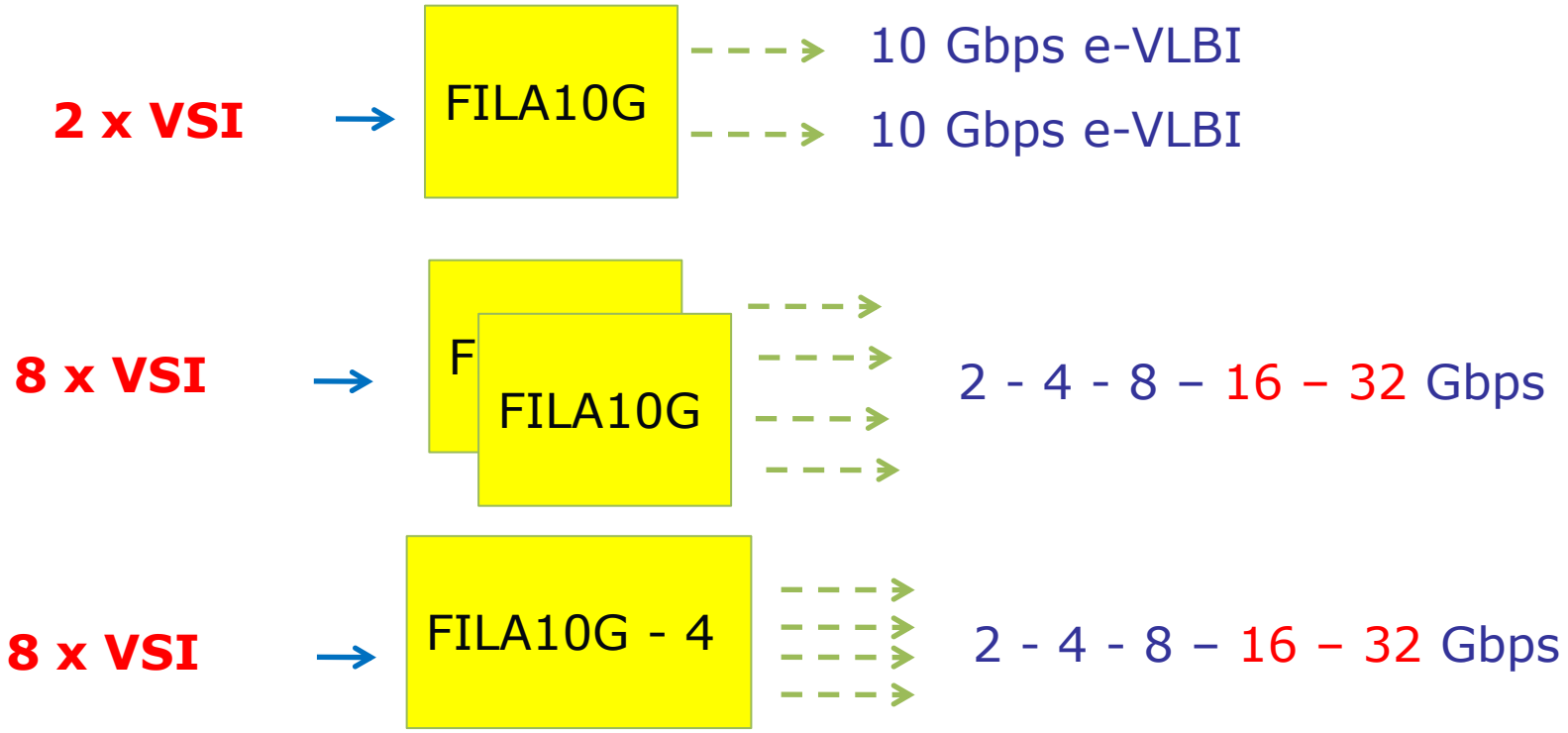


- 2 x VSI --> MK5C = MK5B & 10GE net



Connection examples

- 2 x VSI --> Network

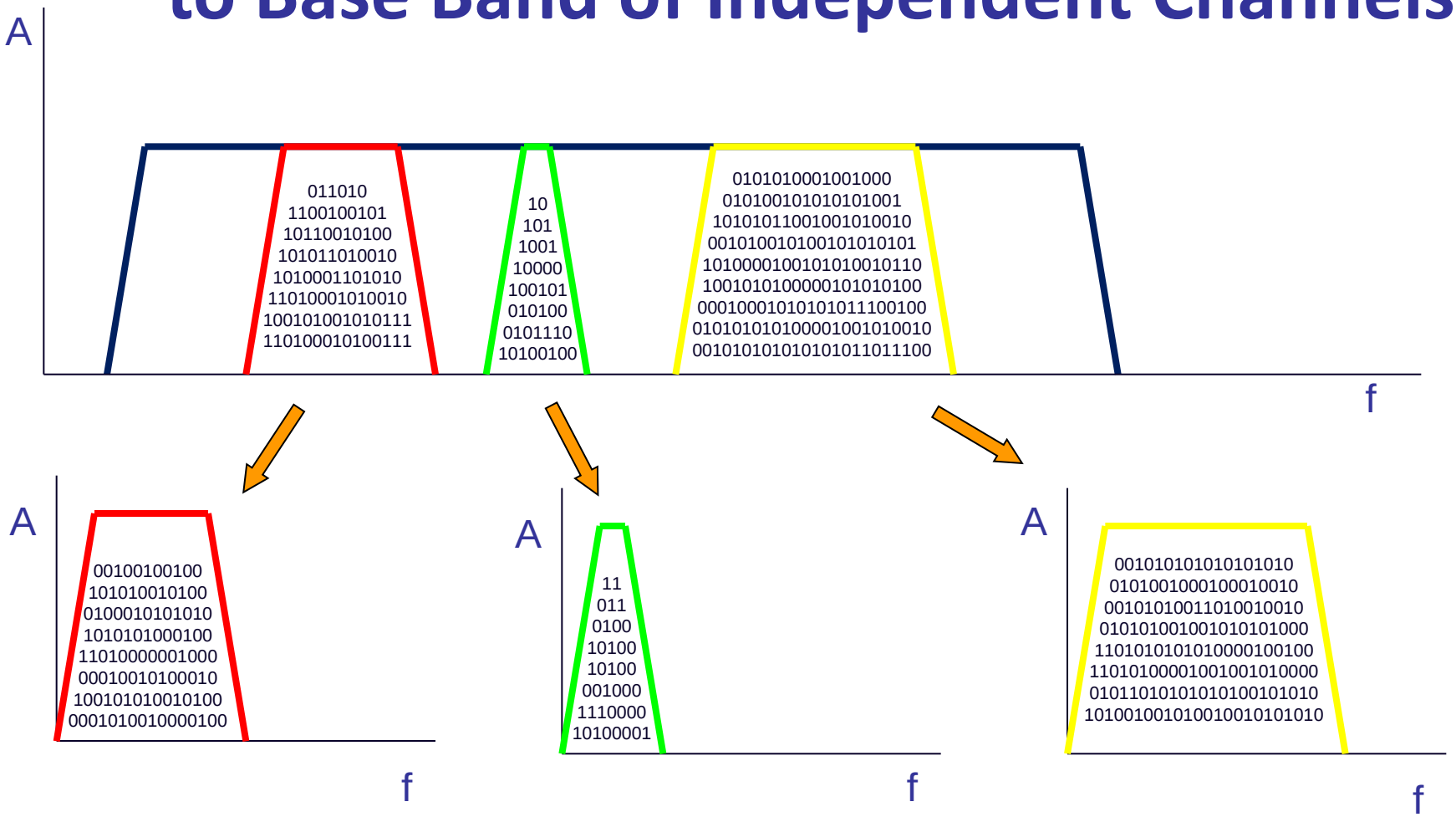


Observing Modes

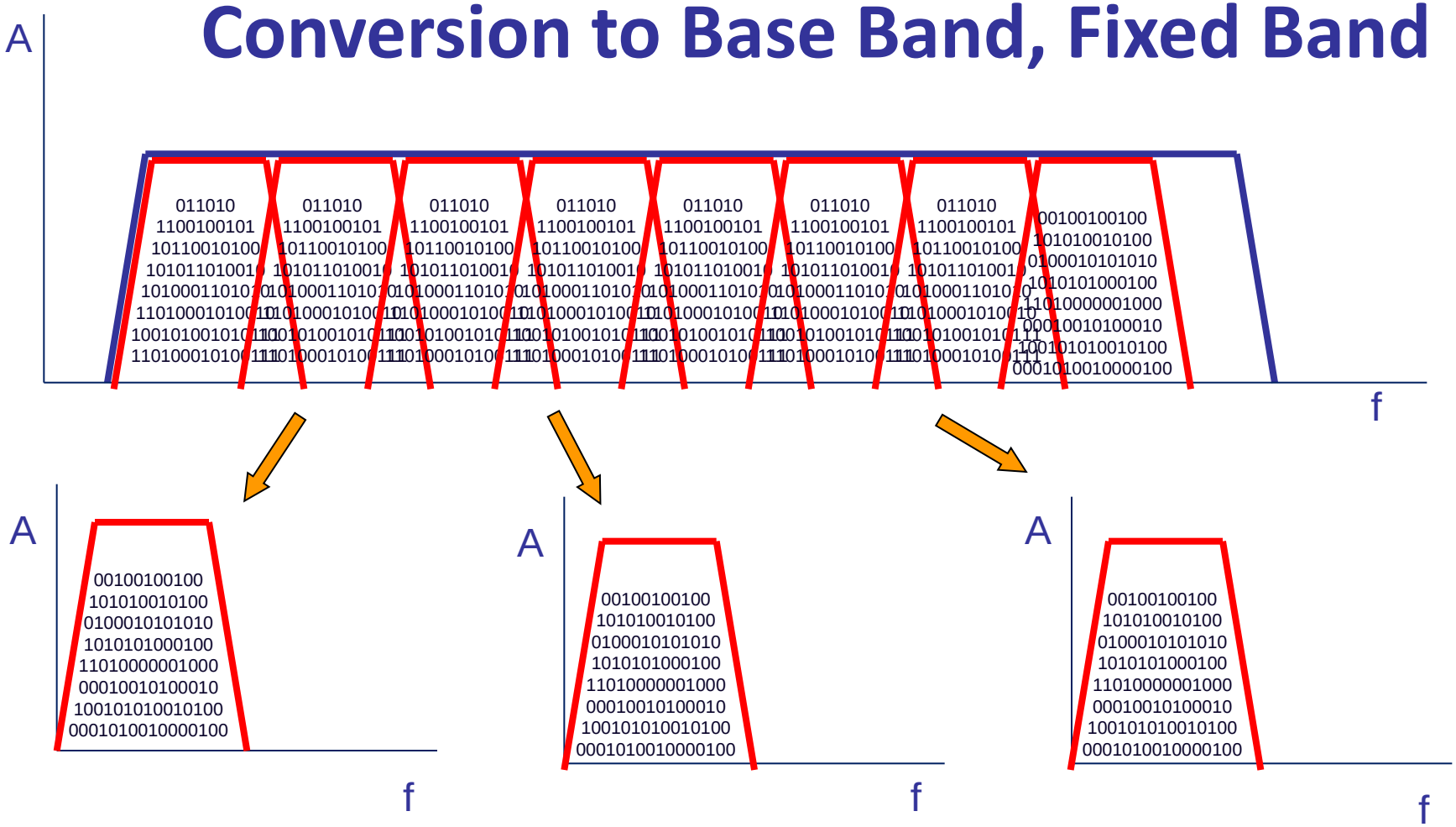
Observing Modes (today)

- **DDC: tunable, channel bandwidth between 1 MHz and 16 MHz, U&L, Continuous cal with 80 Hz synchronization, mode ‘geo’, ’astro’, astro2, ‘w-astro’, ‘lba’, ’test’**
- **PFB: fixed tuning, channel bandwidth 32/64 MHz, all U or L depending on the Nyquist zone**
- **DSC: full 4 x 512/1024 MHz, max 8 x 1024 MHz band direct sampling conversion, all U or L depending on the Nyquist zone**
- **SPECTRA: 4Kch/IF spectrometer, max 32K channels**

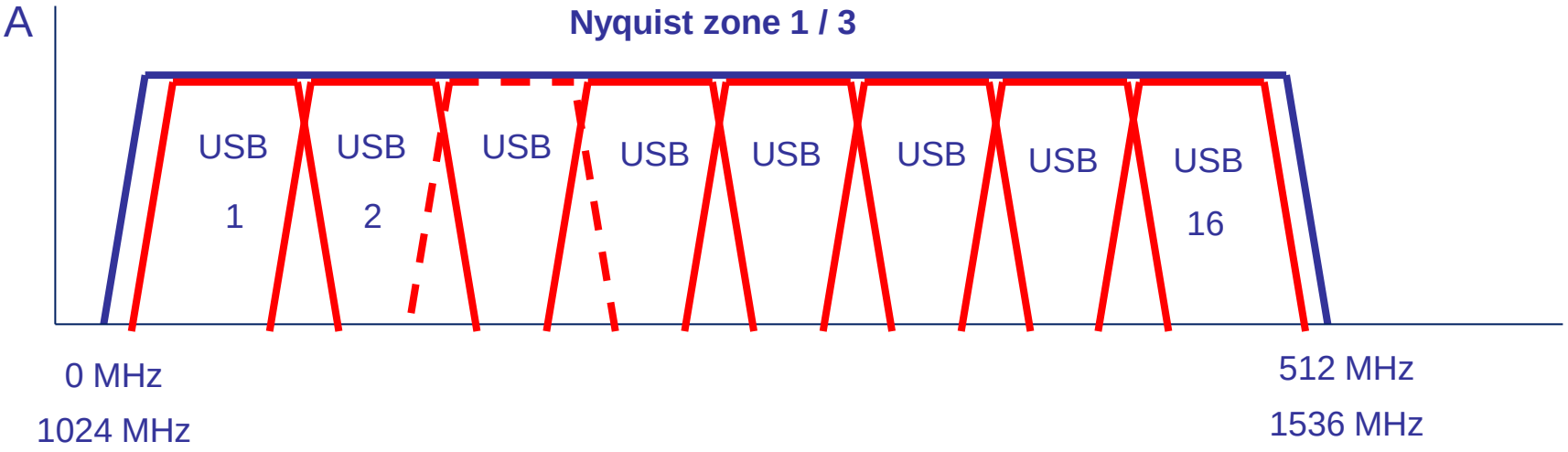
DDC - Digital Down Conversion to Base Band of Independent Channels

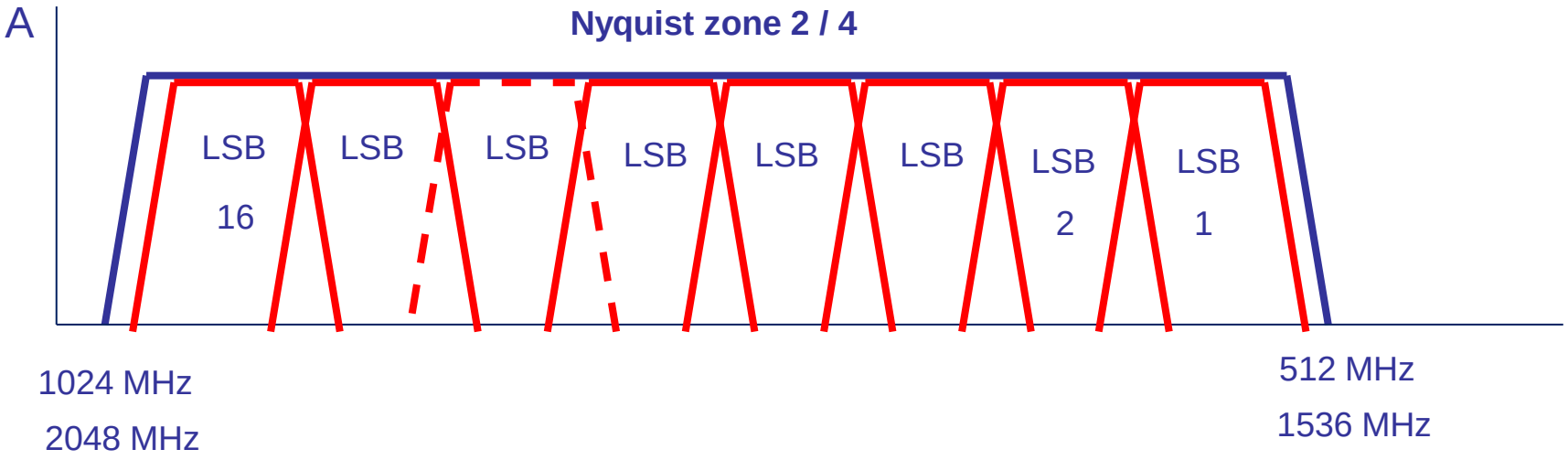


PFB – Polyphase Filter Bank
Conversion to Base Band, Fixed Band

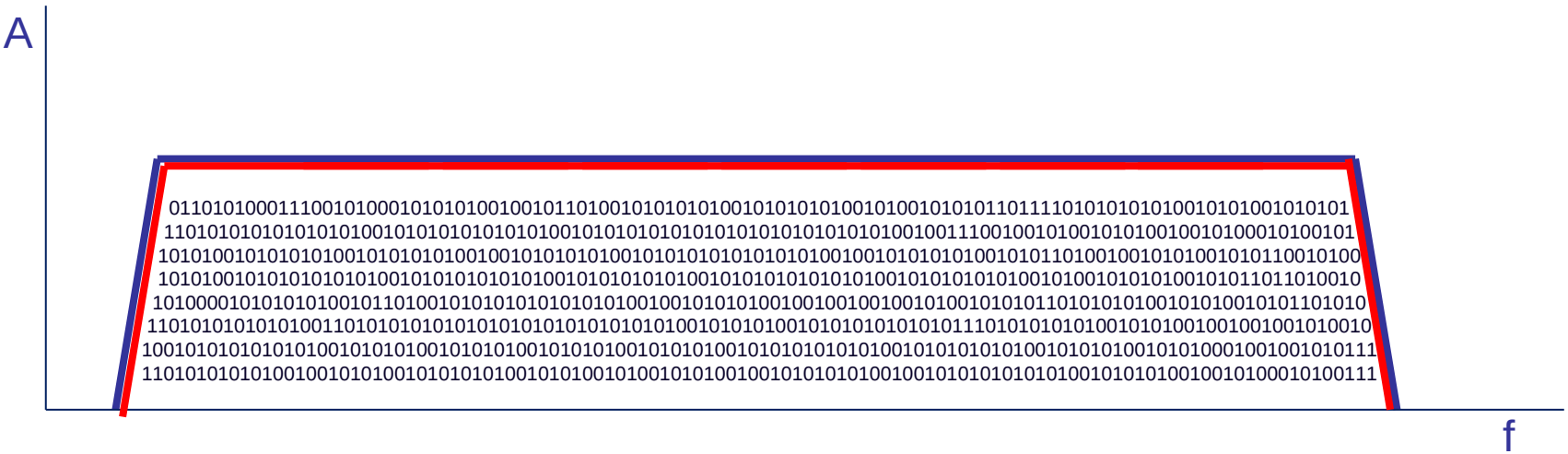


PFB – Polyphase Filter Bank
USB / LSB depends on the Nyquist zone

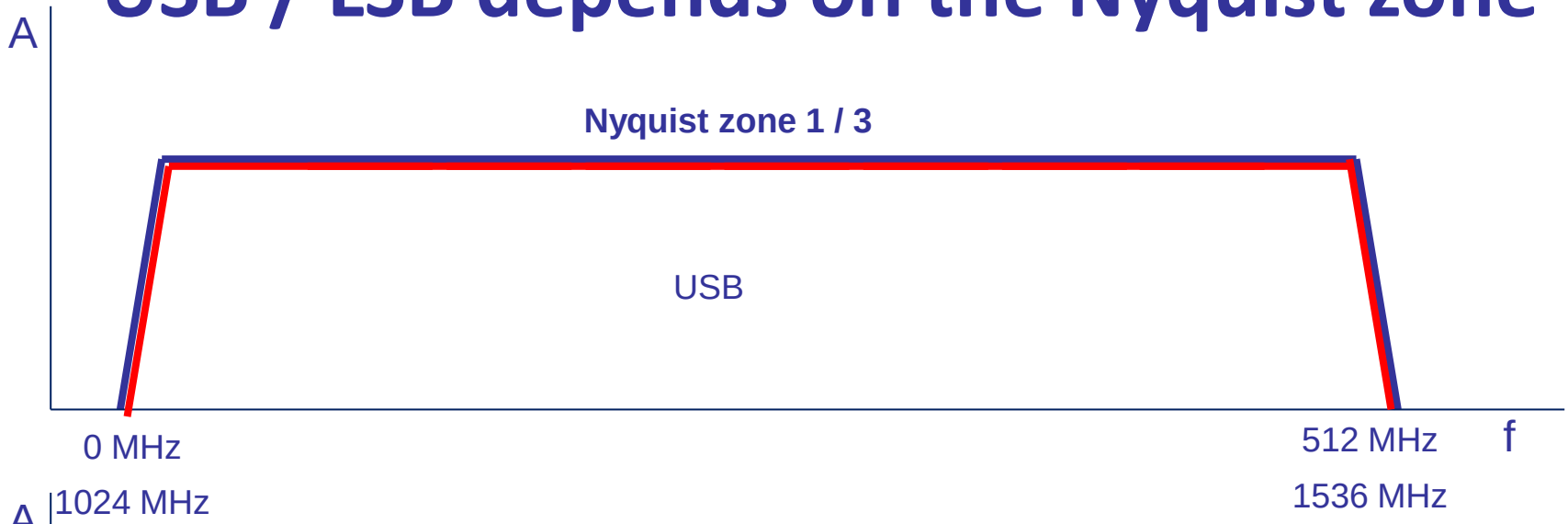


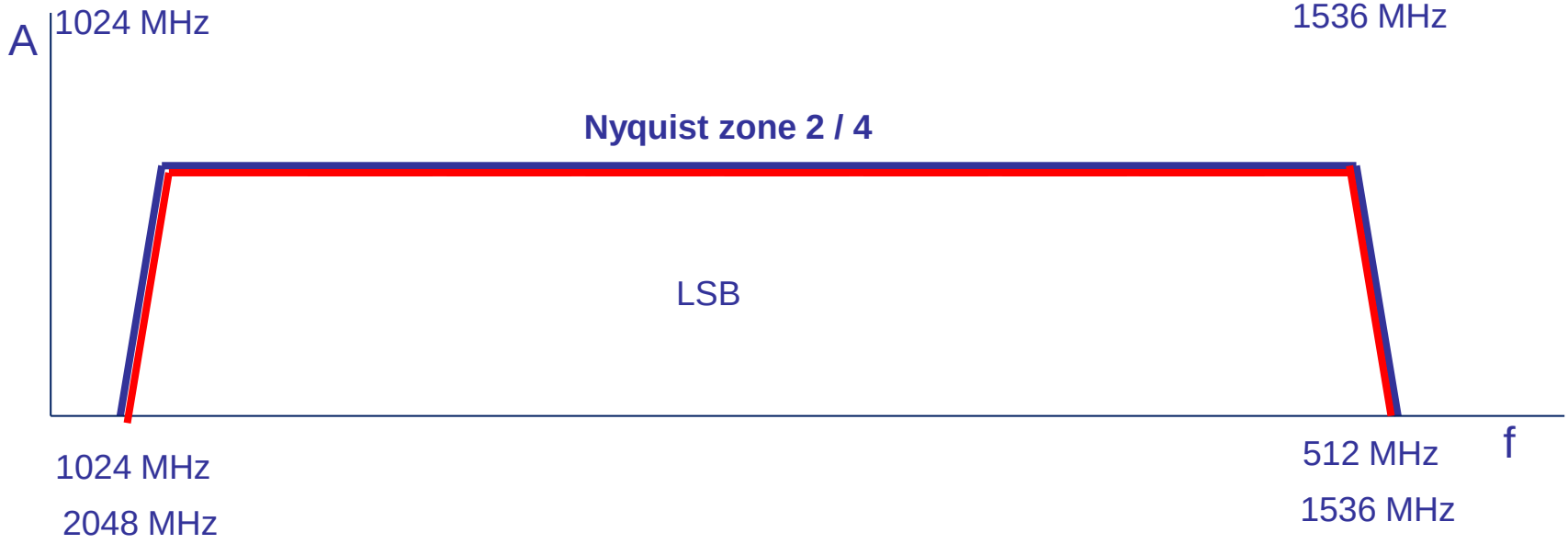


DSC – Direct Single band Conversion
Conversion to Base Band, Full Band



DSC – Direct Single band Conversion
USB / LSB depends on the Nyquist zone





How the observing mode is selected

- **Using a dedicated firmware**
- **Using a dedicated control software**
- **Using a dedicated configuration text file**

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Home

Welcome to the Hat-Lab home page

HAT-Lab s.r.l. is a INAF (Istituto Nazionale di Astrofisica) spin-off company.

The first and main goal is to produce and continue the development of the DBBC (Digital Base Band Converter) system, a digital back-end endorsed by the European VLBI network, and adopted as digital processing unit in the radiotelescopes worldwide for scientific research.

Indeed the system is a very flexible environment used to observe astronomic, geodetic and space science targets with interferometric or single-dish methods.

The wide band and high data rate processing of the DBBC allows to significantly improve the radiotelescope sensitivity and perform high precision data handling for a more accurate scientific result.

INAF ira

EUROPEAN VLBI NETWORK

14139
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Number of Categories: 6

 DDC - Tunable 16 bbc — Files: 4

 BASE - General — Files: 4

 FILA10G - 10G Ethernet — Files: 2

 PFB - Polyphase 16 bands — Files: 3

SPECTRA - Spectrometer — Files: 1

 Technical Notes — Files: 10

search...

Files Structure

(under Windows XP)

- **C:\DBBC\bin → control software**
- **C:\DBBC\doc → manuals**

- **C:\DBBC_CONF\ → configuration text files**
- **C:\DBBC_CONF\FilesDBBC → firmware**

Software

- **General:**

BASE Package

c:\DBBC\bin\DBBC client v3.exe (general client)

c:\DBBC\bin\clock1024.exe (CAT2 1024)

c:\DBBC\bin\clock2048.exe (CAT2 2048)

c:\DBBC\bin\ad9858.exe (CAT1)

c:\DBBC\bin\power.exe (on-off hardware)

c:\DBBC\bin\agc_if.exe (CoMo Unica3 test)

c:\DBBC\bin\agc_if_unica4.exe (CoMo Unica4 test)

DDC

Software on socket

- **DDC :**

c:\DBBC\bin\DBBC2 Control DDC v104.exe (server)

c:\DBBC_conf\dbbc_config_file_104.txt

c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v104.bit

c:\DBBC\doc\DBBC2 DDC command set v104.pdf

c:\DBBC_conf\ dbbc_config_file_104.txt

Example:

1 dbbc2_ddc_v101.bit 597.00 8 ←the first number is indication of ADB1|2, in this case ADB1 is on
1 dbbc2_ddc_v101.bit 597.00 8 IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v101.bit 597.00 8 If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v101.bit 597.00 8 The second parameter is the firmware file name to be used.
2 dbbc2_ddc_v101.bit 597.00 8 The third 2 dbbc2_ddc_v101.bit 597.00 8 and fourth parameters are frequency and bandwidth respectively.
2 dbbc2_ddc_v101.bit 597.00 8 Each Core2 board supports 4 bbcs so if not present 0 has to be inserted in four lines
2 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 597.00 8
0 dbbc2_ddc_v101.bit 597.00 8
0 dbbc2_ddc_v101.bit 597.00 8
0 dbbc2_ddc_v101.bit 597.00 8
0 dbbc2_ddc_v101.bit 597.00 8
1 fila10g_v2_1.bit ← if a FILA10G is installed set first version 1 (with ACE), second version (without ACE 2), otherwise 0
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0 ← phase calibration values
CAT2 1024 ← CAT1|2 and sampling frequency

DDC: running **DBBC2 Control DDC v104.exe**

```
DBBC Control net_v101.exe
core 1  1       dbbc2_v101.bit conf. file       130.990000 lo freq      4 bw filter
core 2  1       dbbc2_v101.bit conf. file       140.990000 lo freq      4 bw filter
core 3  1       dbbc2_v101.bit conf. file       170.990000 lo freq      4 bw filter
core 4  1       dbbc2_v101.bit conf. file       230.990000 lo freq      4 bw filter
core 5  1       dbbc2_v101.bit conf. file       340.990000 lo freq      4 bw filter
core 6  1       dbbc2_v101.bit conf. file       420.990000 lo freq      4 bw filter
core 7  1       dbbc2_v101.bit conf. file       470.990000 lo freq      4 bw filter
core 8  1       dbbc2_v101.bit conf. file       490.990000 lo freq      4 bw filter
core 9  0       dbbc2_v101.bit conf. file       192.990000 lo freq      4 bw filter
core 10 0       dbbc2_v101.bit conf. file       207.990000 lo freq      4 bw filter
core 11 0       dbbc2_v101.bit conf. file       217.990000 lo freq      4 bw filter
core 12 0       dbbc2_v101.bit conf. file       247.990000 lo freq      4 bw filter
core 13 0       dbbc2_v101.bit conf. file       267.990000 lo freq      4 bw filter
core 14 0       dbbc2_v101.bit conf. file       272.990000 lo freq      4 bw filter
core 15 0       dbbc2_v101.bit conf. file       100.990000 lo freq      4 bw filter
core 16 0       dbbc2_v101.bit conf. file       200.990000 lo freq      4 bw filter
FiLa10G 0

Reconfigure? y/n  _
```

after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe or Field System**

DDC Mode Commands and Form Table (see documents)

DDC settings and optimization

- Phase optimization: to be performed with a synthesizer and the dedicated command at the system installation.

  To be repeated after a hardware modification in the stack or transportation. Periodically as a general check.
- Amplitude optimization: to be performed using phase cal tones injected in the receiver and ‘bpcal’ software from Haystack.

  To be repeated after a hardware modification, new receivers, etc. Periodically as a general check.
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check.

PFB

Software on socket

- **PFB :**

c:\DBBC\bin\ DBBC2 Control PFB v15.exe (server)

c:\DBBC_conf\ dbbc_poly_config_file_15.txt

c:\DBBC_conf\FilesDBBC\ dbbc2_pfb_v15.bit

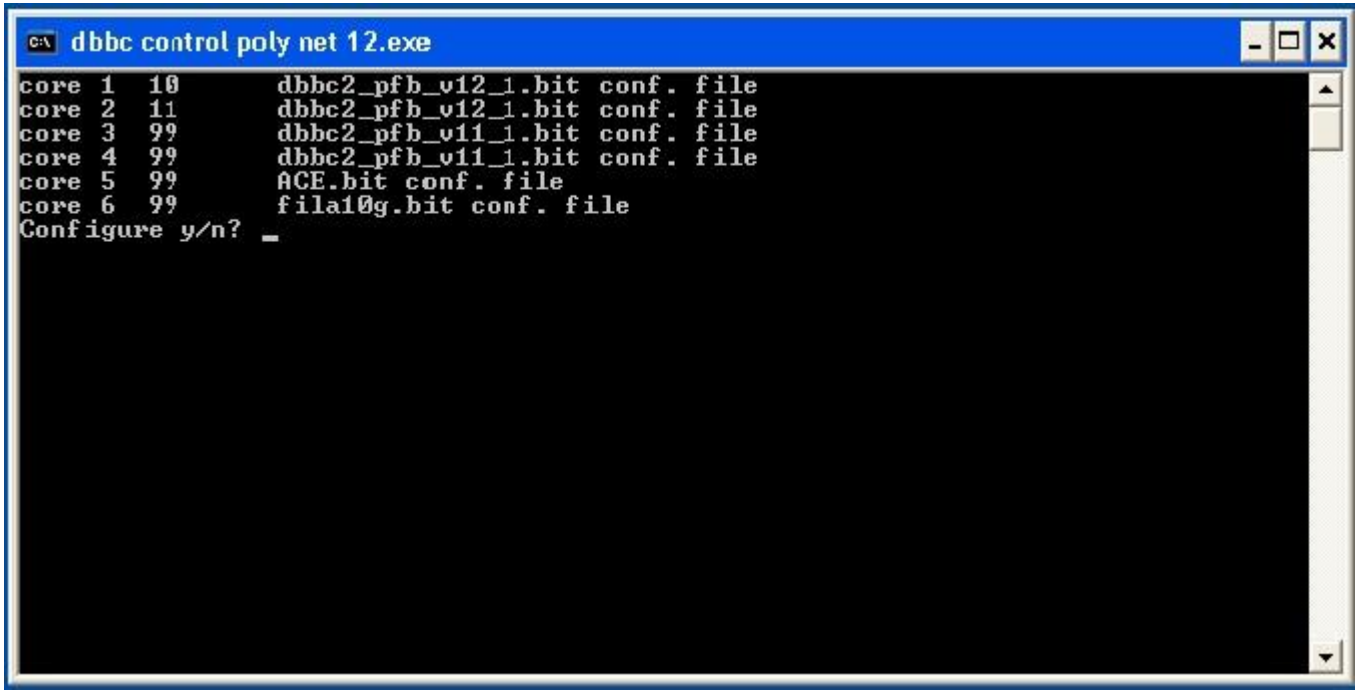
c:\DBBC\doc\ DBBC2 PFB command set v15.pdf

c:\DBBC_conf\ dbbc_poly_config_file_15.txt

Example:

```
10 dbbc2_pfb_12.bit   ←the first number is indication of ADB1|2, in this case ADB1 is on IFa
21 dbbc2_pfb_12.bit     and ADB2 on IFB, etc. The second number is the Core2 board address.
12 dbbc2_pfb_12.bit     If no Core2 is inserted in the first and second column put 99.
13 dbbc2_pfb_12.bit     Third parameter is the firmware file name to be used.
99 ACE.bit            ← do not modify here
99 fila10g.bit        ← if a FILA10G with ACE is installed in the DBBC JTAG chain set 01,
                        if a FILA10G without ACE is installed set 02,  otherwise 99
1 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 58000               ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0           ←  phase calibration values
CAT1 1024             ←  CAT1|2 and sampling frequency
```

PFB: running **DBBC2 Control PFB v15.exe**



after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe or Field System**

PFB Mode Commands, Form Table , PFB Frequencies (see documents)

PFB settings and optimization

- Phase optimization: to be performed with a synthesizer and the dedicated command at the system installation.

  Values could be different by the DDC ones.

  To be repeated after a hardware modification in the stack or transportation. Periodically as a general check.
- Amplitude optimization: to be performed using phase cal tones injected in the receiver and 'bpcal' software from Haystack.

  To be repeated after a hardware modification, new receivers, etc. Periodically as a general check.
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check.

DSC

Software on socket

- **Implemented inside PFB software and firmware with ‘dbbcmode=full’, so again:**

c:\DBBC\bin\ DBBC2 Control PFB v15.exe (server)

c:\DBBC_conf\ dbbc_poly_config_file_15.txt

c:\DBBC_conf\FilesDBBC\ dbbc2_pfb_v15.bit

c:\DBBC\doc\ DBBC2 PFB command set v15.pdf

DSC settings and optimization

- Phase optimization: PFB recommendations
- Amplitude optimization: PFB recommendations
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check
- Dedicated test software developed and running on MK5B+

SPECTRA

Software on socket

- **SPECTRA :**

c:\DBBC\bin\ DBBC2 Control SPC v1.exe (server)

c:\DBBC_conf\ dbbc_spc_config_file_1.txt

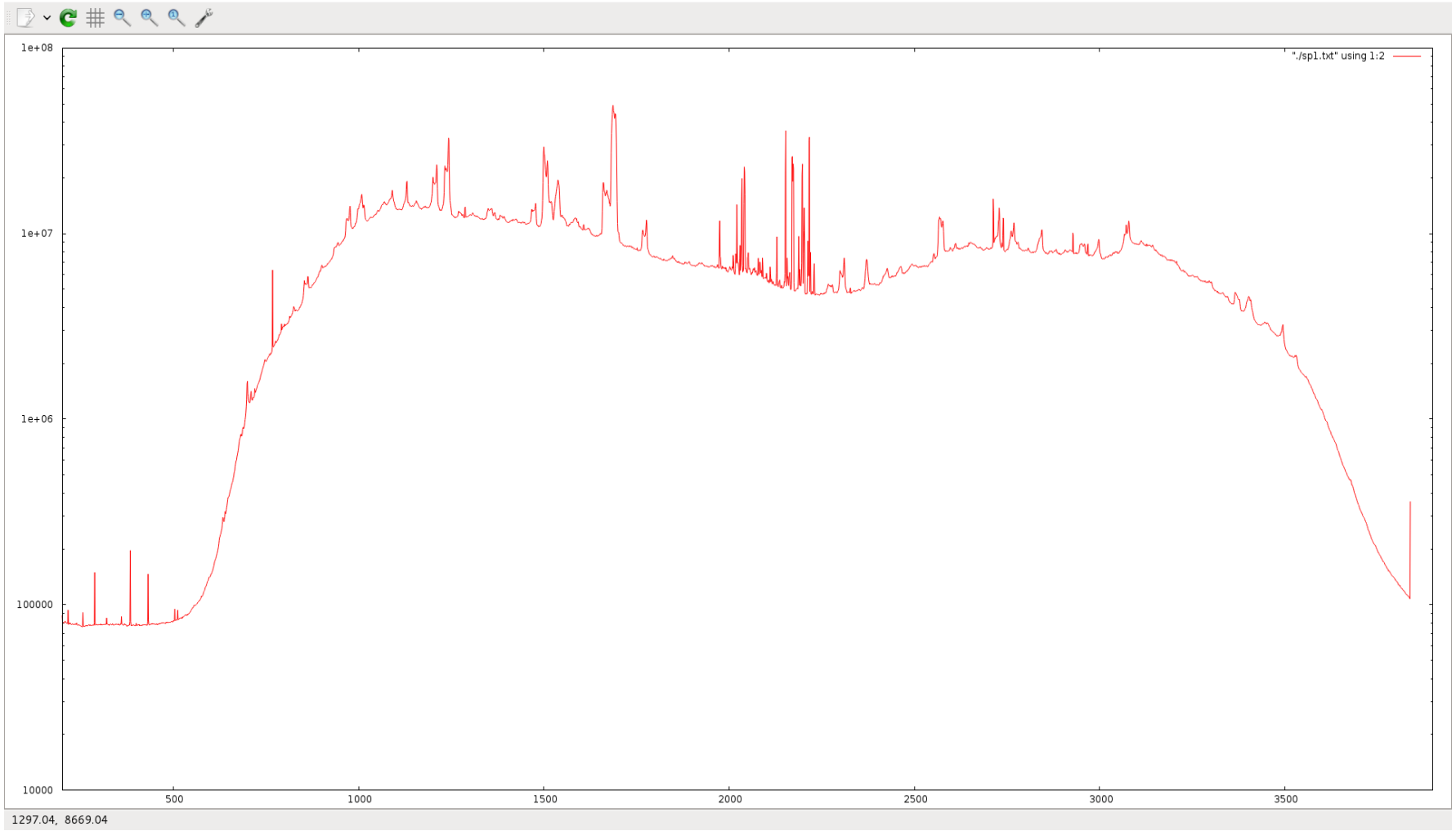
c:\DBBC_conf\FilesDBBC\ dbbc2_spc_v1.bit

c:\DBBC\doc\ DBBC2 SPC command set v1.pdf

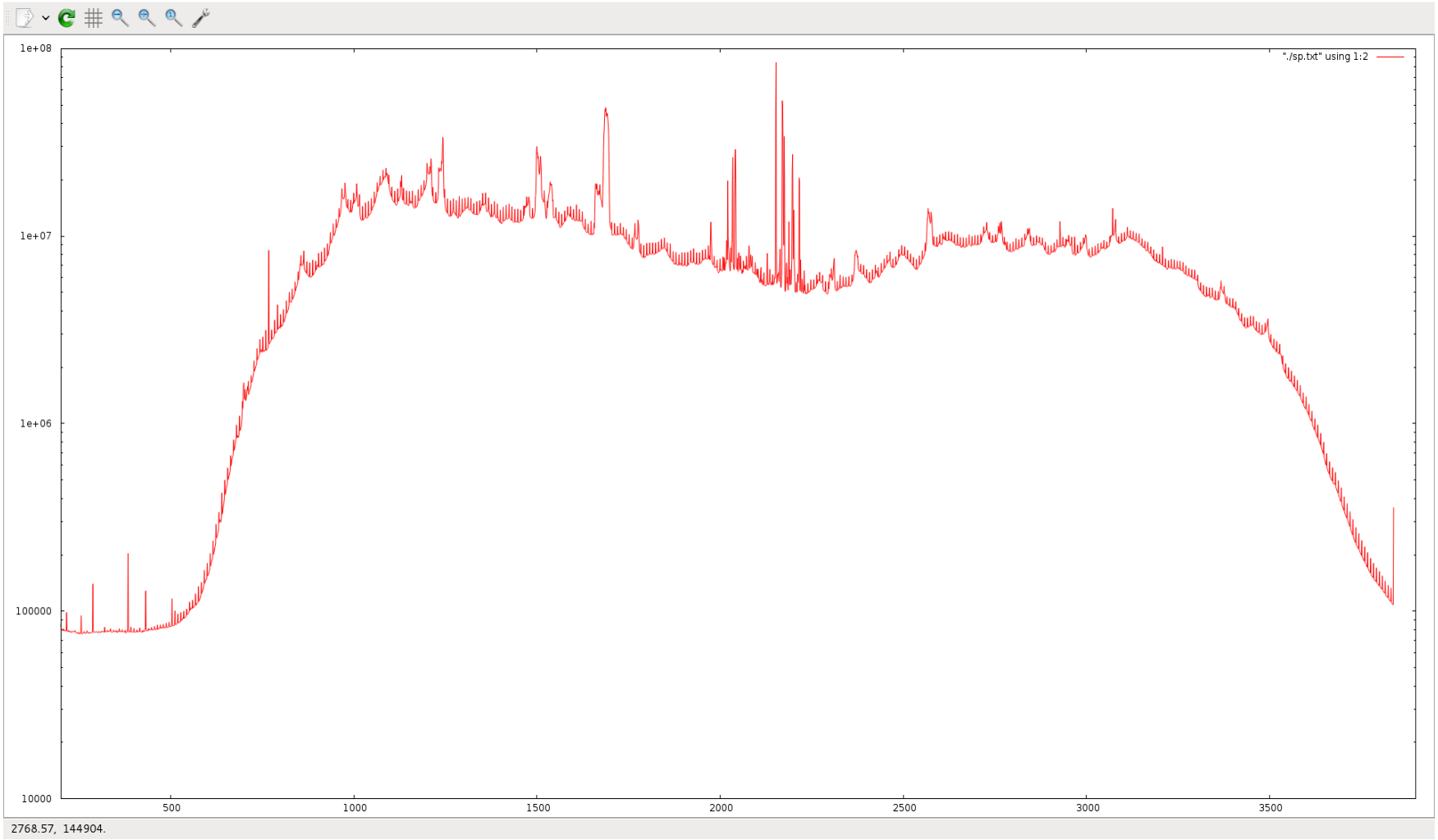
c:\DBBC_conf\ dbbc_spectra_config_file_1.txt

```
Example:
10 dbbc2_pfb_12.bit   <- the first number is indication of ADB1|2, in this case ADB1 is on IFa
21 dbbc2_pfb_12.bit    and ADB2 on IFB, etc. The second number is the Core2 board address.
12 dbbc2_pfb_12.bit    If no Core2 is inserted in the first and second column put 99.
13 dbbc2_pfb_12.bit    Third parameter is the firmware file name to be used.
99 ACE.bit            <- do not modify here
99 fila10g.bit        <- if a FILA10G with ACE is installed in the DBBC JTAG chain set 01,
                         if a FILA10G without ACE is installed set 02, otherwise 99
1 58000               <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 58000                <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 58000                <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 58000               <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 58000               <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 58000               <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 58000               <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 58000               <- no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0           <- phase calibration values
CAT1 1024             <- CAT1|2 and sampling frequency
```

Noto L band cal tones off



Noto L band cal tones on



How to set the FILA10G

- Download the firmware is automatically made by the DDC/PFB control software
- In the FILA-SA a script file can be used with the additional included Xilinx Jtag programmer
- Communication is through serial port or Ethernet in the stand-alone version
- Commands available (see document)
- VDIF packet size setting (see document)
- Script files can be used for block of commands (see batch)

- **FILA10G Files:**

c:\DBBC\bin\ timesyncFILA10G.exe (MK5B time set)

c:\DBBC\bin\ vdif_timesyncFILA10G.exe (VDIF time set)

c:\DBBC\bin\ sendstr.exe (serial communication)

c:\DBBC_conf\FilesDBBC\ fila10g_v2.bit

c:\DBBC\doc\ DBBC2 FILA10G Command set v2.pdf

Note: a program to sync with a NTP server is required (ex. NetTimeSetup-314.exe)

Commands integrated in DDC v105 (under way) and PFB v15

fila10g = synch, [YYYY-MM-DD: hh:mm:ss]
Synchronize the FILA10G clock .
Arbitrary time optionally set.

fila10g = time
Reports FILA10G time and difference with respect to DBBC-PC time in seconds.

fila10g = mode, format, source, packetsize
format => 5b | vdif
source => vsi1 | vsi2 | vsi1-2 |
vsi1 and vsi2 are 2 Gbps modes, vsi1-2 is 4 Gbps mode
| test-2-0 | test-2-1 | test-2-b | test-2-t | test-4-0 | test-4-1 | test-4-b | test-4-t |
'test-2-x' are 2Gbps modes, 'test-4-x' are 4Gbps modes
packetsize => data frame size in single thread mode: 64,80,128,160,200,256,320,400,512,640,800,1000,1024,
1280,1600,2000,2048,2560,3200,4000, 4096,5000,5120,6400,8000,8192
on both eth0 and eth1 ports.

fila10g = start | stop
Run or stop the 10G packets on both eth0 and eth1 ports

fila10g = cmd = direct command
direct command is sent as recognized by the FILA10G.

DBBC3 - Full digital VLBI2010

DBBC3

- Project supported by EU Radionet3
- Partners:

  INAF – Italy

  MPIfR - Germany

  OSO – Sweden
- Starting date July 2012, duration 3 years

Twofold implementation

- Astronomic VLBI: 32Gbps EVN, mmVLBI
- Geodetic VLBI: VLBI2010

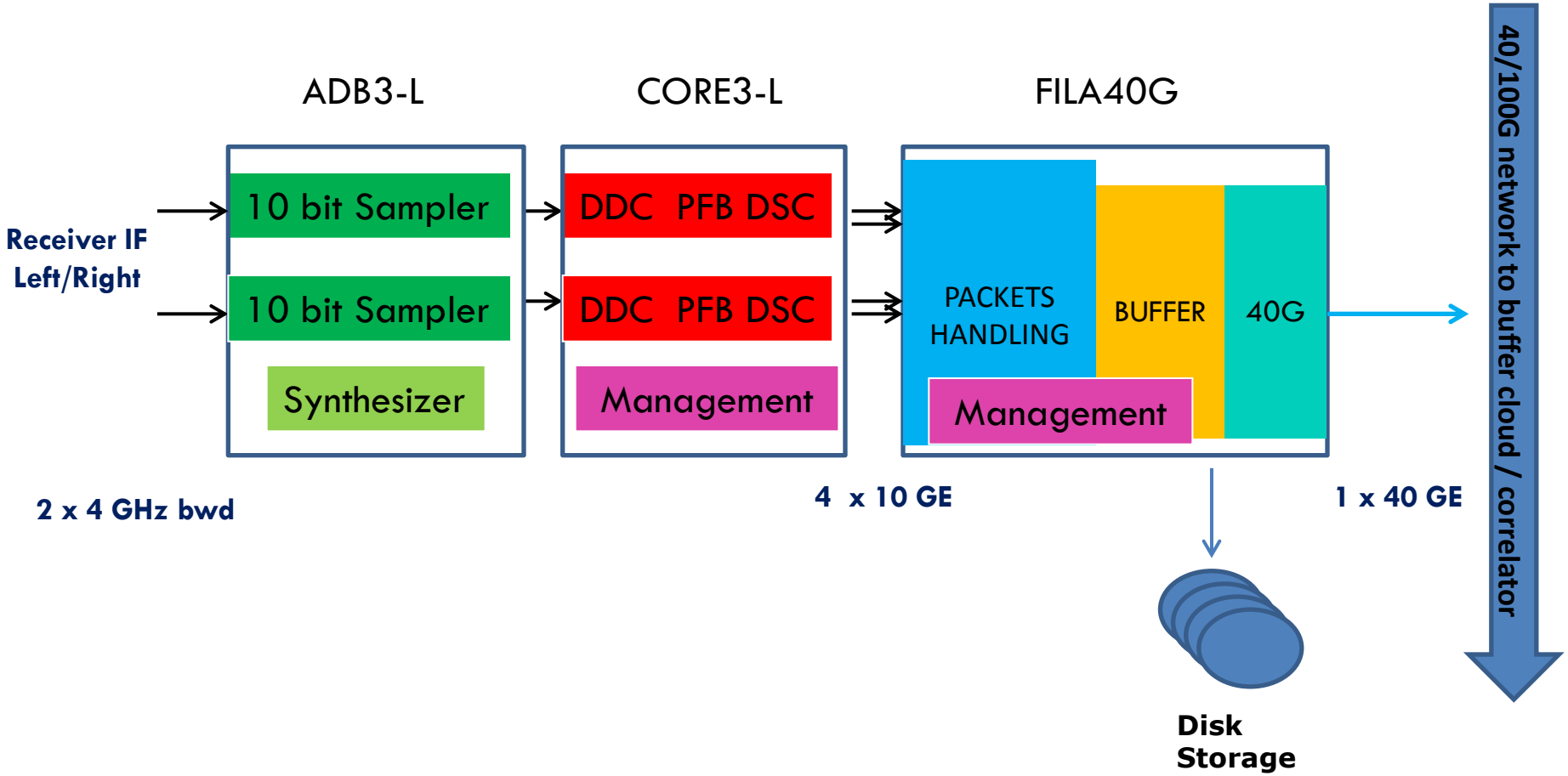
DBBC3 General Performance for EVN

- Number of Input IF: **1 - 4**
- Instantaneous bandwidth ea. RF: **>=4 GHz**
- Sampling representation: **10 bit**
- Processing capability: max **10 TMACS** (multiplication-accumulation per second)
- Output: **VDIF Ethernet packets, >=32Gbps**
- Compatibility with existing DBBC environment

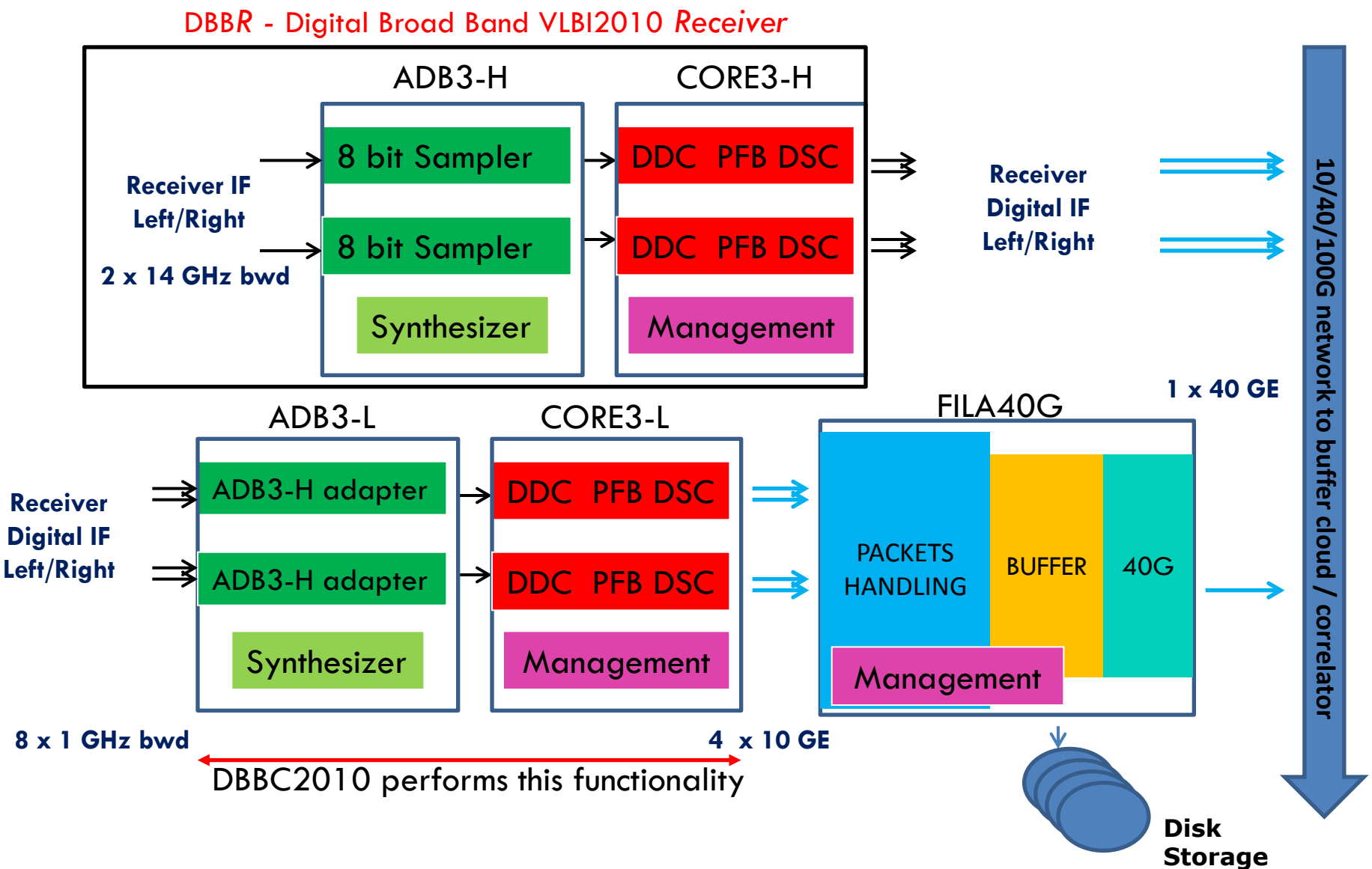
DBBC3 General Performance for VLBI2010

- Number of Input IF: **1 - 4**
- Instantaneous bandwidth ea. RF: =1**4-16 GHz**
- Sampling representation: **8 bit**
- Processing capability: max **10 TMACS** (multiplication-accumulation per second)
- Output: **VDIF Ethernet packets, >=64Gbps**
- Compatibility with existing DBBC environment

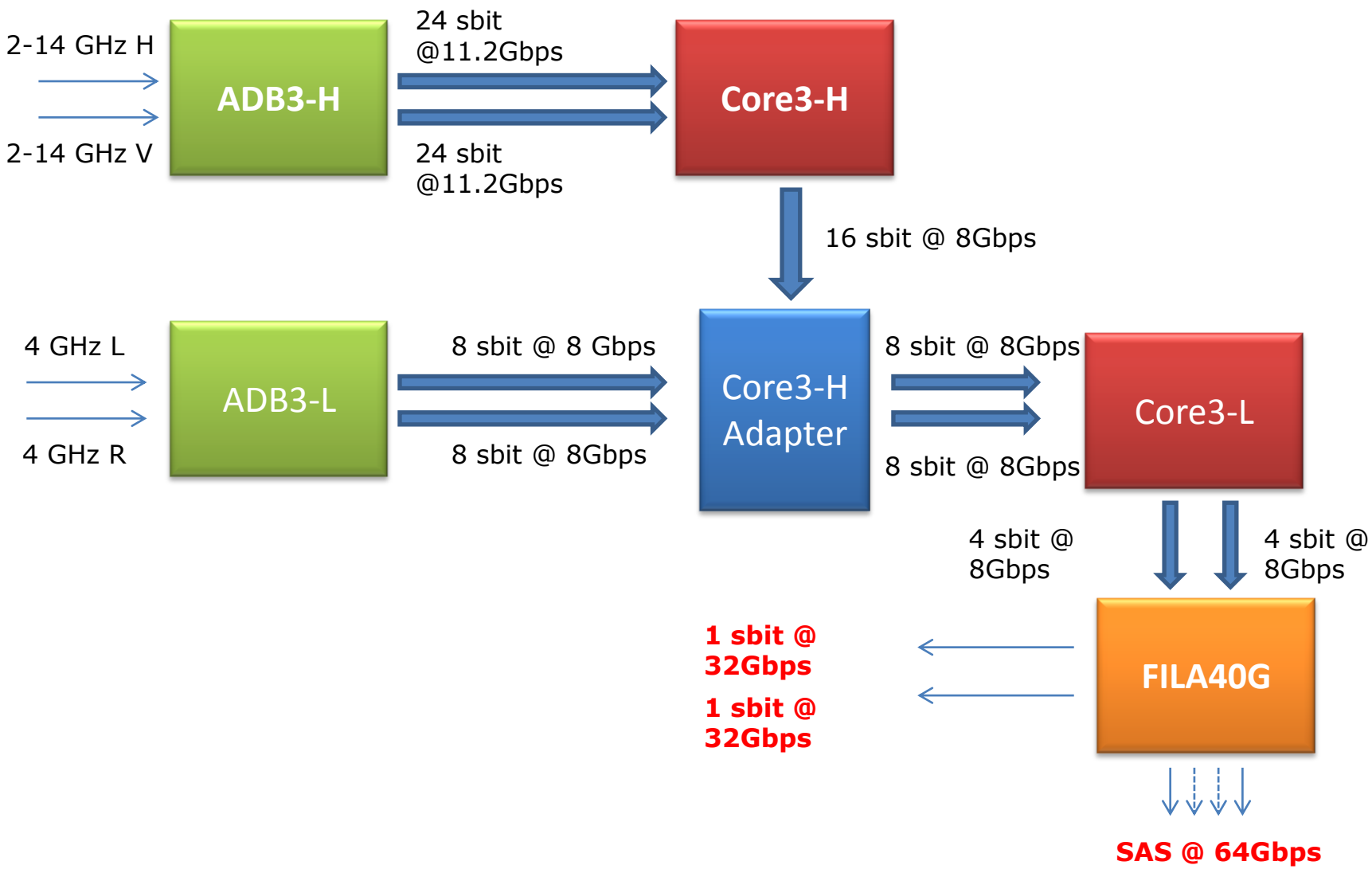
Typical DBBC3 Architecture for EVN



Typical DBBC3 Architecture for VLBI2010



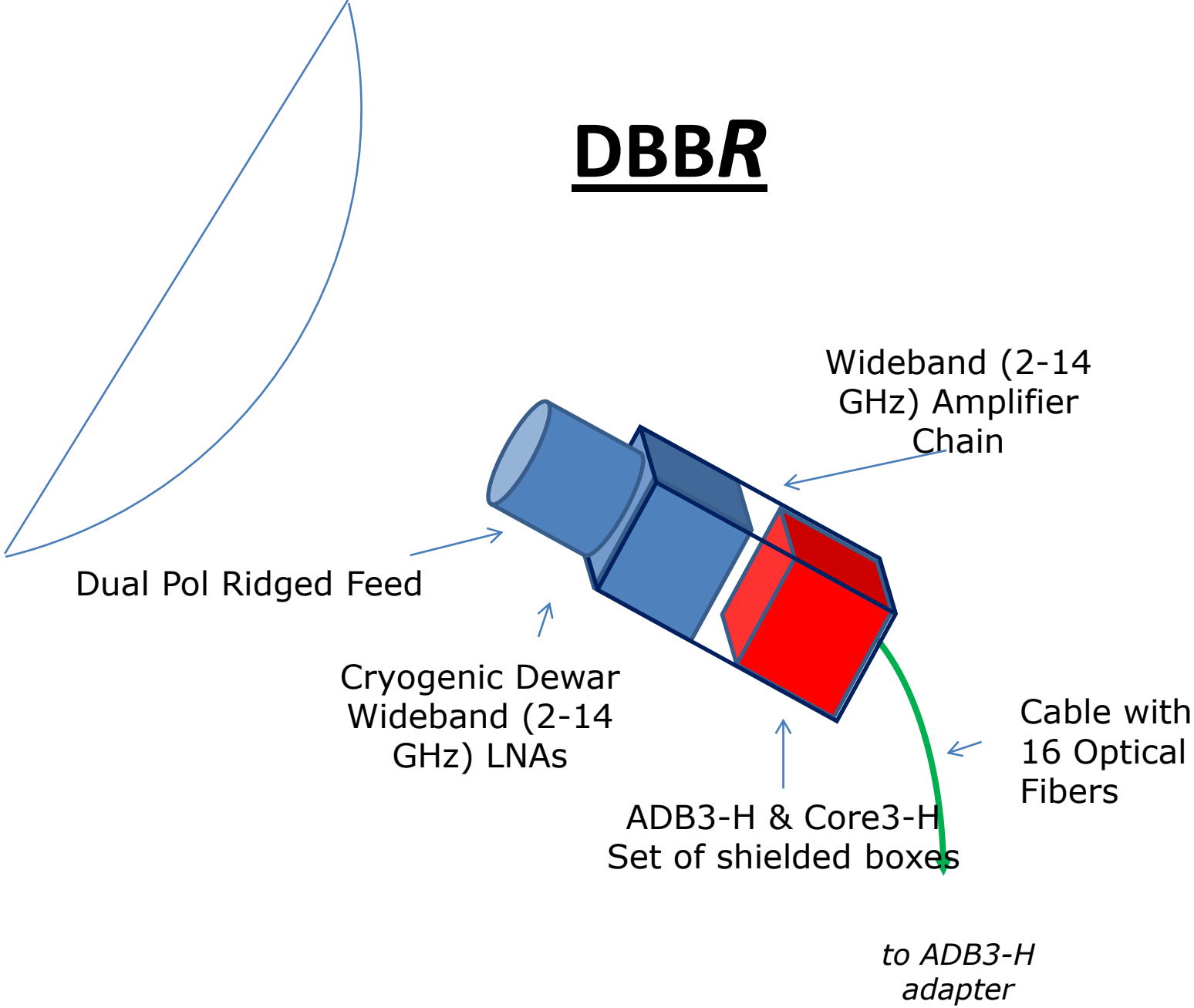
DBBC3 Architecture Data Flow



DBB*R* – Digital Broad Band *R*eceiver

- Fully digital receiver at sky frequency
- Feed developed in Italy
- Feed and LNA at cryogenic temperature
- Sky frequency sampling
- Digital down conversion
- Output based on Digital Optical Link

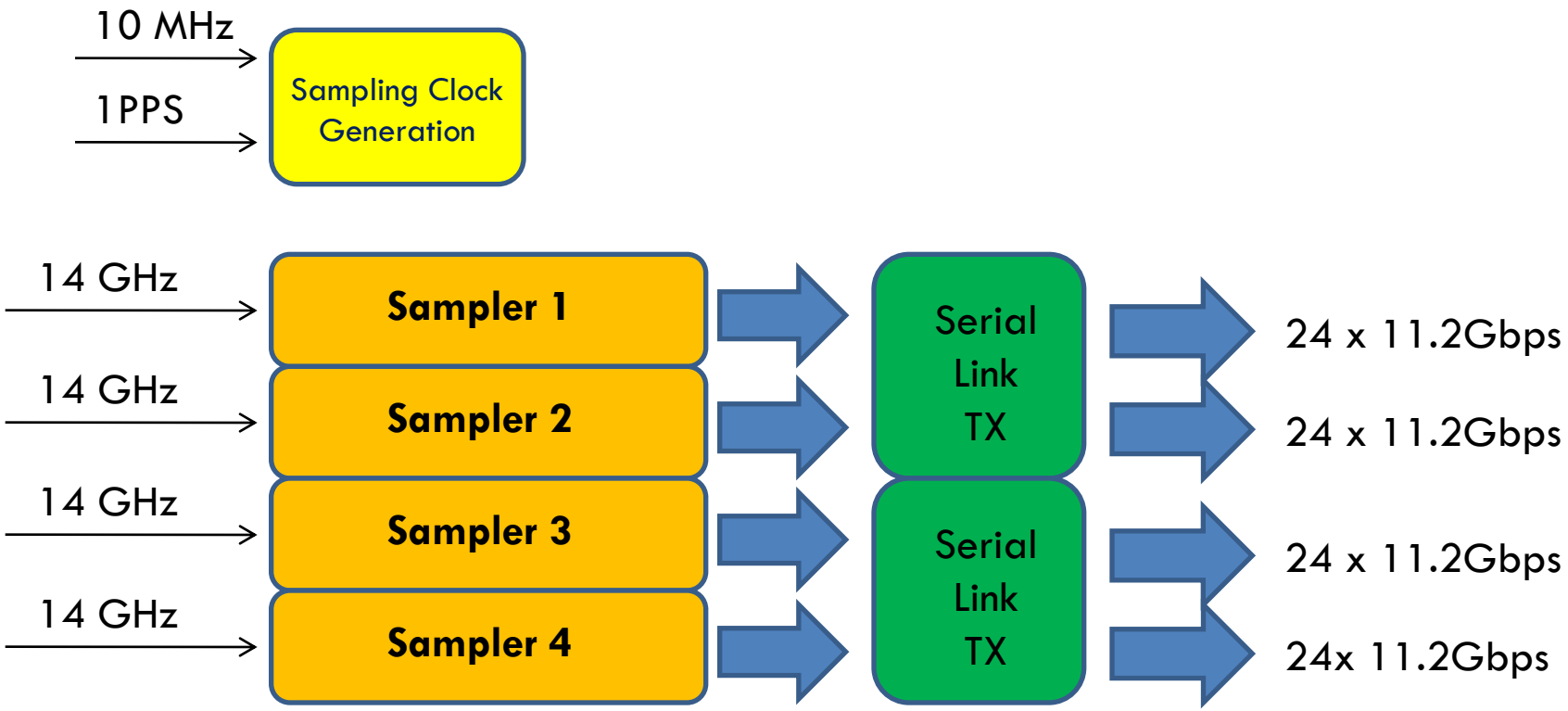
DBB*R*


Wideband (2-14 GHz) Amplifier Chain
Dual Pol Ridged Feed
Cryogenic Dewar Wideband (2-14 GHz) LNAs
Cable with 16 Optical Fibers
ADB3-H & Core3-H Set of shielded boxes
to ADB3-H adapter

ADB3-H General Performance

- **ADB3-H:**
  Number of IFs: **4**
  Equivalent Sample Rate ea. IF: **28.672 GSps**
  Instantaneous bandwidth ea. IF: **14.336 GHz**
  Sampling representation: **8 bit**
- Real Sampling
- Compatibility with existing DBBC environment
- **Engineers samples available, commercial devices expected in fall 2013**

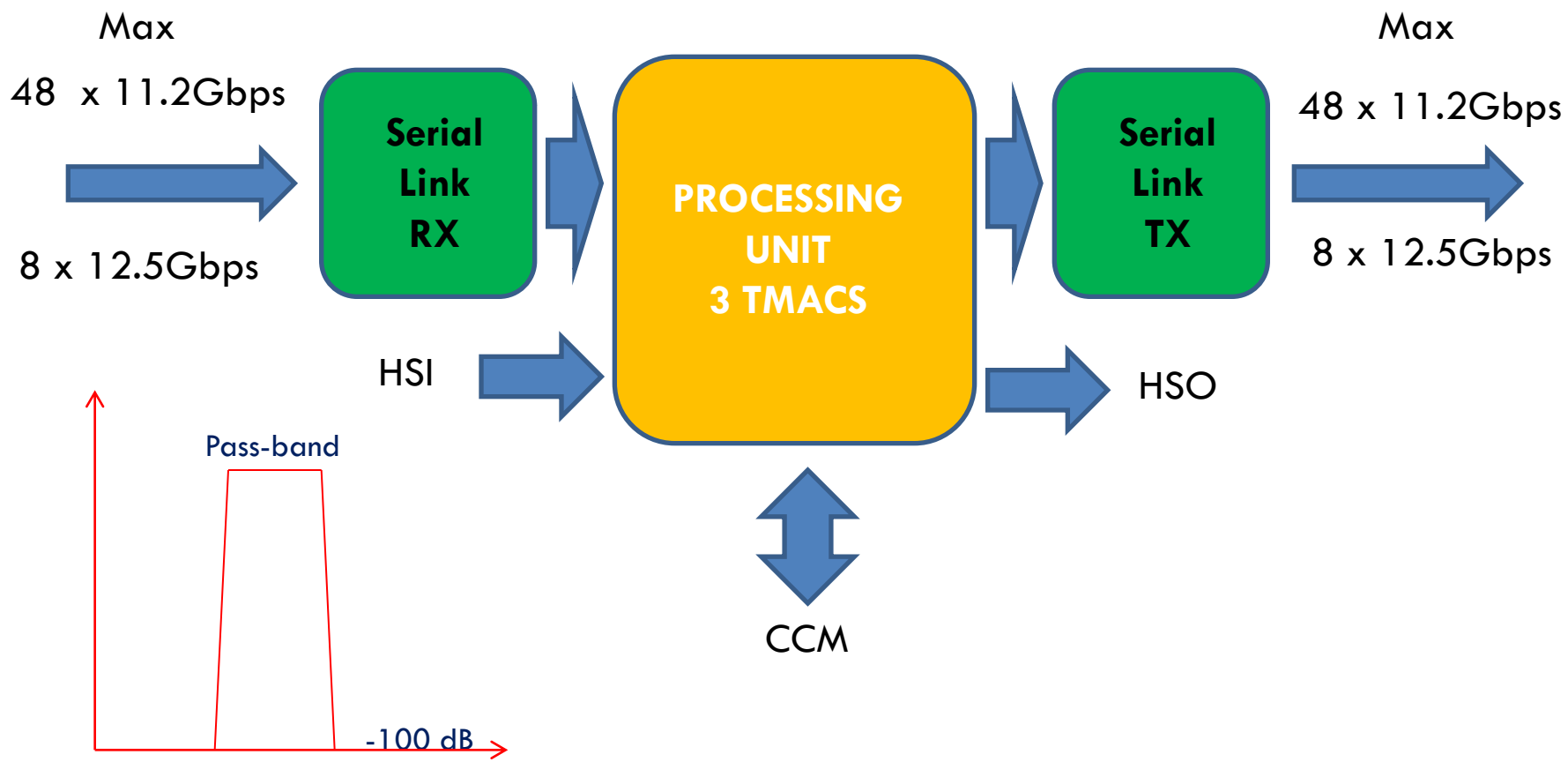
ADB3-H Sampler



CORE3-H General Performance

- **Core3-H**
- Number of Input: **max 48 serial links 11.2Gbps**
- Number of Output: **max 48 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **max 5 TMACS** (multiplication-accumulation per second)
- Processing capability: **WB-DDC, WB-PFB, DCS**
- Output: **VDIF Ethernet packets, >=32Gbps**
- Compatibility with existing DBBC environment
- **DDC Firmware under development on prototype board**

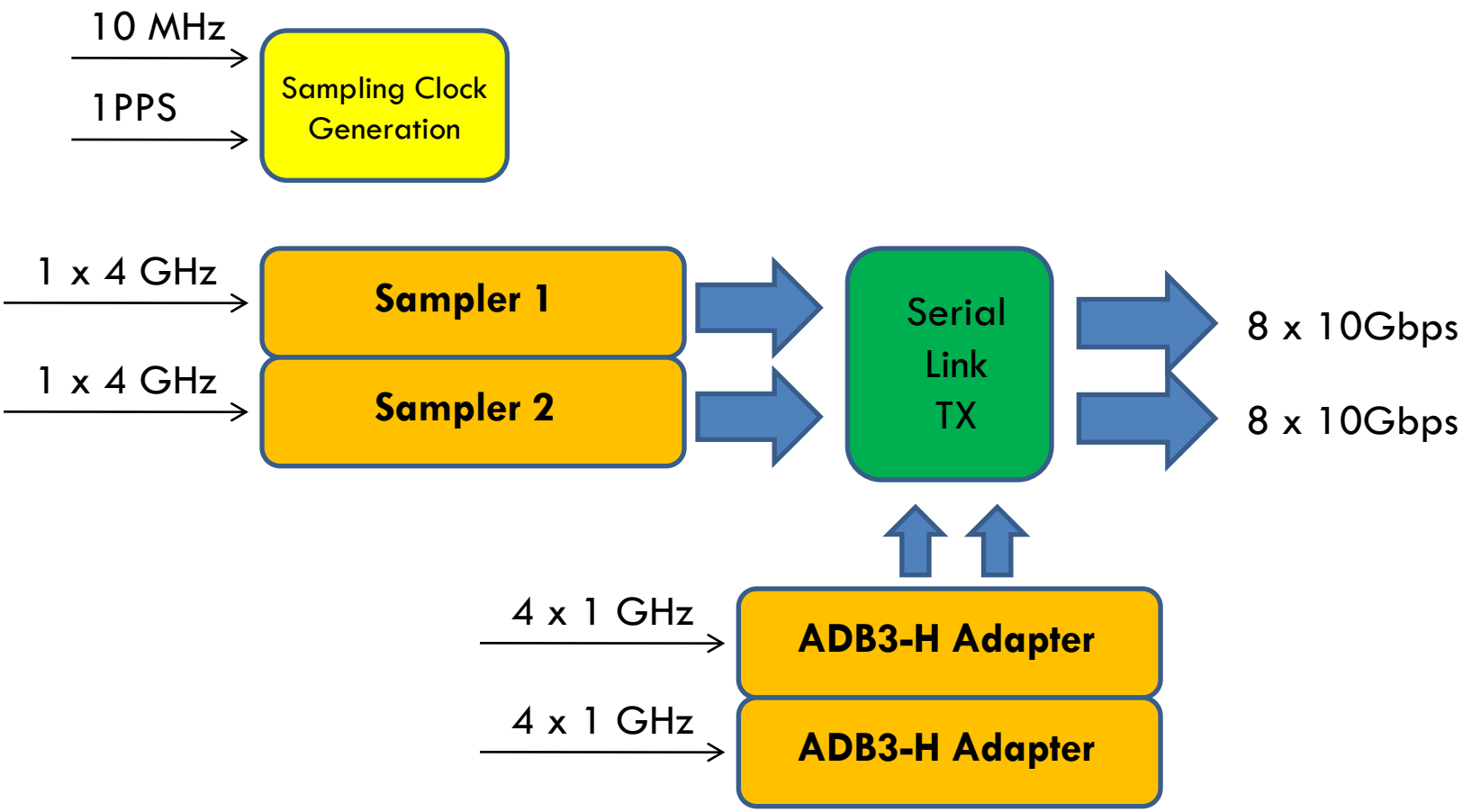
CORE3-H


Max
48 x 11.2Gbps
8 x 12.5Gbps
Serial Link RX
PROCESSING UNIT 3 TMACS
Serial Link TX
Max
48 x 11.2Gbps
8 x 12.5Gbps
HSI
HSO
CCM
Pass-band
-100 dB

ADB3-L General Performance

- **ADB3-L:**
  Number of IFs: **2**
  Equivalent Sample Rate ea. IF: **8 GSps**
  Instantaneous bandwidth ea. IF: **4 GHz**
  Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC environment
- **First prototype successfully tested, pcb project of the module ready**

ADB3-L Sampler



CORE3-L General Performance

- **Core3-L**

  Number of Input: **max 16 serial links 10Gbps**

  Number of Output: **max 16 serial links 10Gbps**

  Input Sampling Representation: **8-10 bit**

  Processing capability: **max 3 TMACS**

  (multiplication-accumulation per second)

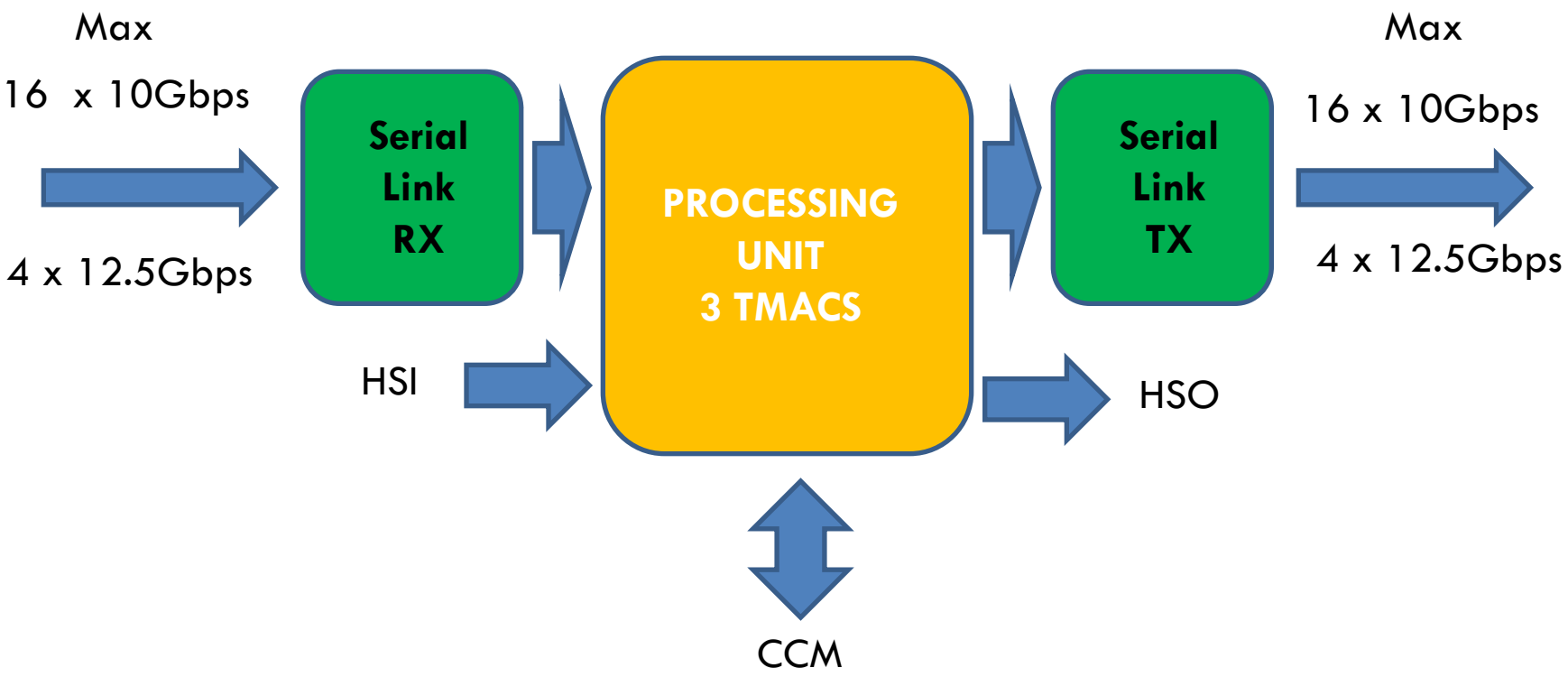
  Processing capability: **WB*-DDC, WB*-PFB, DCS**

  Output: **VDIF Ethernet packets, >=32Gbps**

  Compatibility with existing DBBC environment
- **Same device of Core3-H in reduced pin-out version**
- **DDC and PFB Firmware to be derived from the current DBBC2**

* Wide band

CORE3-L

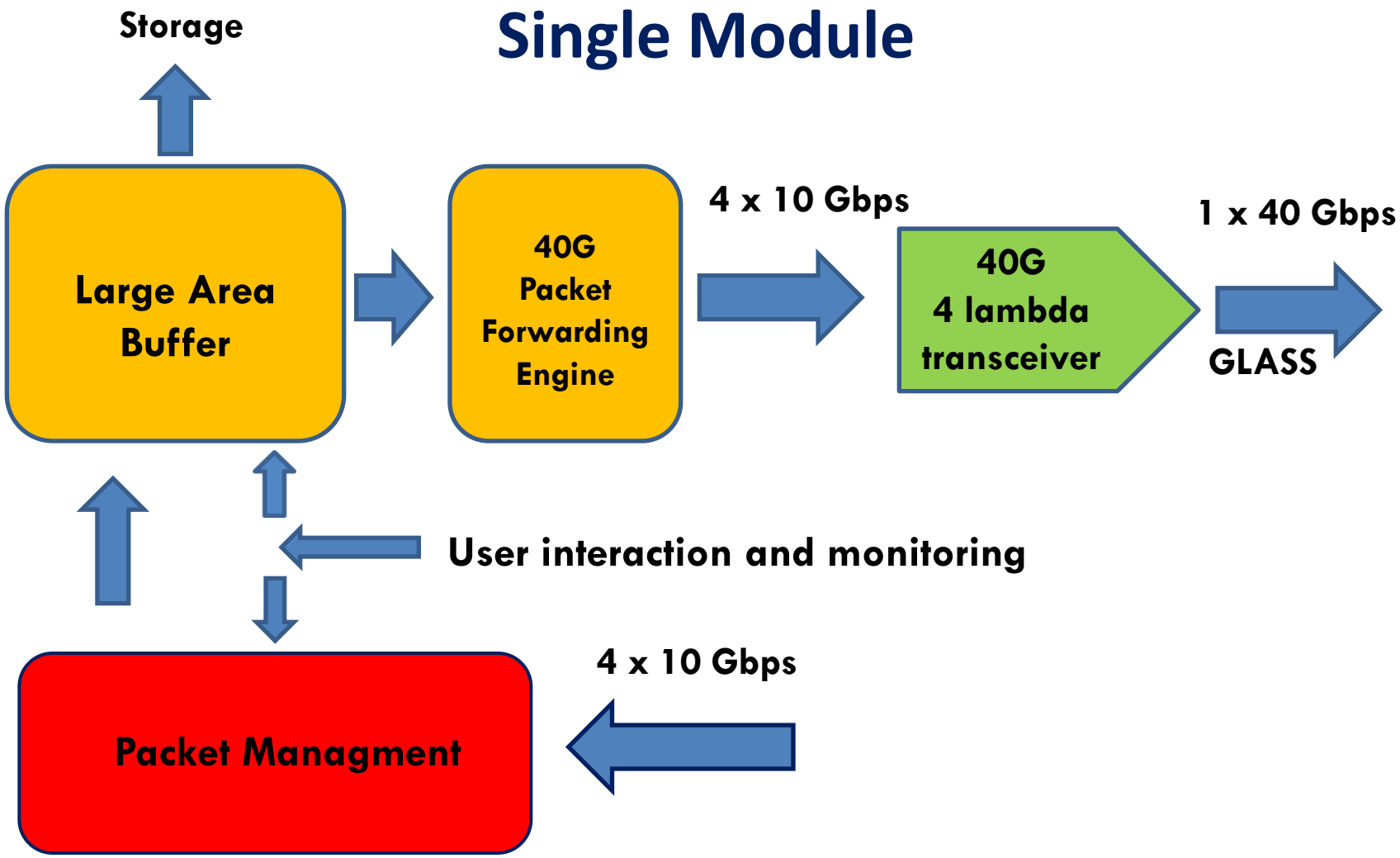

Max
16 x 10Gbps
4 x 12.5Gbps
Serial Link RX
PROCESSING UNIT 3 TMACS
Serial Link TX
Max
16 x 10Gbps
4 x 12.5Gbps
HSI
HSO
CCM

FILA40G Single Module General Performance

- Serial Link Input: = **4 x 10Gbps**
- Serial Link Output: = **1 x 40Gbps**
- Packets manipulating capability (filtering, pulsar gating, burst mode, etc.)
- Packets forwarding capability (different correlator nodes, different correlator sites, etc)
- Packets monitoring capability
- SAS ports for storage
- **Project under definition**

FILA40 Architecture

Single Module



FILA 40G Single Module