DBBC Developments

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DBBC (Digital Base Band Converter) family overview:

- VLBI back-ends
- VLBI network shifters
- VLBI data buffers
- VLBI digital receivers
- VLBI synthesis arrays

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DBBC Back-ends evolution

DBBC1 2004 - 2008

in: 4 x IF-512MHz

out: **DDC** 16 x bbc (1-2-4-8-16MHz)@32MHz

0.512/1.024 Gbps

DBBC2 2007 – today

in: 4 x IF-512/1024MHz

out: **DDC** 16 x bbc (1-2-4-8-16-32MHz)@32/64MHz

PFB 4 x 16 x (32-64 MHz)@64/128MHz

4.096/8.192 Gbps

DBBC2010 2009 – today

in: 8 x IF – 512/1024MHz

out: **PFB** / **DSC** **16.384/32.768 Gbps**

DBBC Back-ends evolution

DBBC3L (-2L2L) 2014 - today

in: 2 x IF-4096 / 4 x IF-2048 / 8 x IF-1024

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

16/32 Gbps

DBBC3L (-4L4H) 2014 - today

in: 4 x IF-4096 / 8 x IF-2048 / 16 x IF-1024

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

16/32/64 Gbps

DBBC Back-ends evolution

DBBC3L (-8L8H) 2014 - today

in: 8 x IF-4096 / 16 x IF-2048 / 32 x IF-1024 MHz

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

16/32/64/128 Gbps

DBBC3H 2016

in: 4 x IF-14336 MHz

out: **DDC** 1-2-4-8-16-32-64-128-256-512-1024 MHz

PFB 32-64-128-256-512-256-512-1024 MHz

DSC 1024-2048-4096-8192-14336 MHz

16/32/64/128/229 Gbps

DBBC3 is then dedicated to:

Astronomy

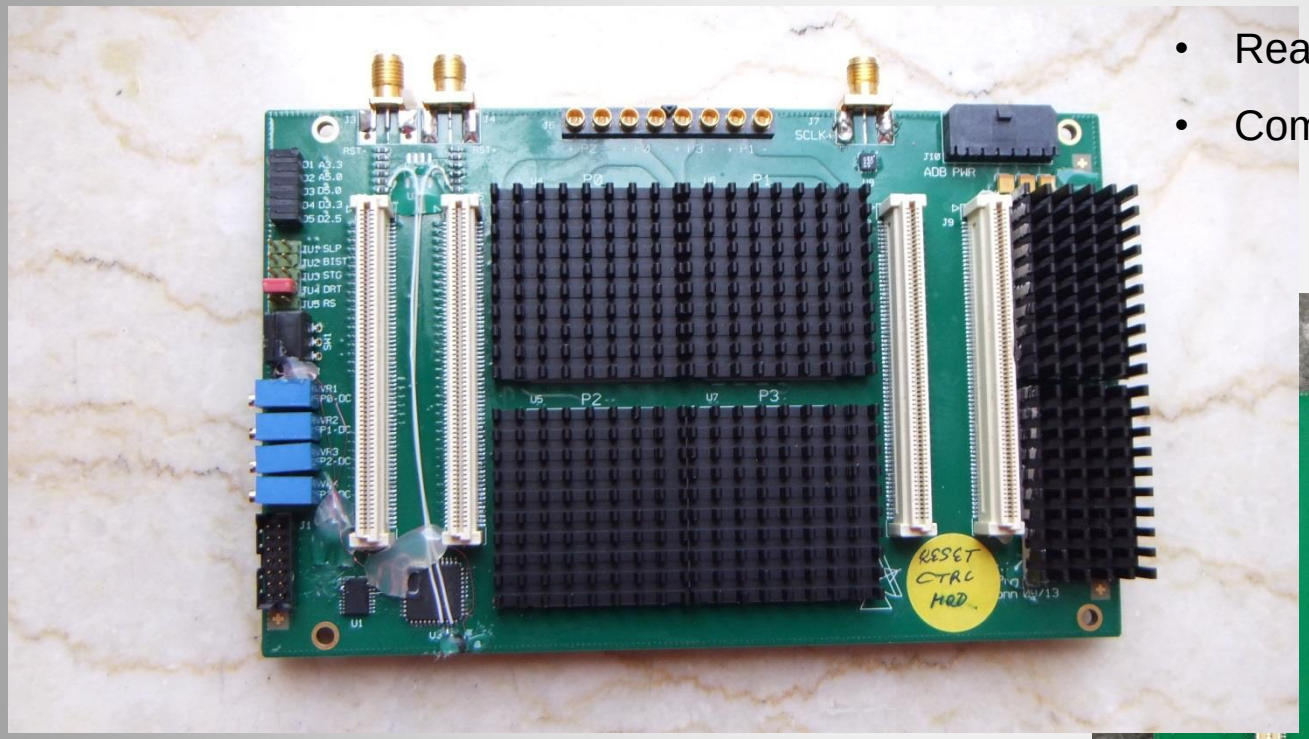
- **EVN wide-band VLBI backend**
- **EHT (Event Horizon Telescope)**

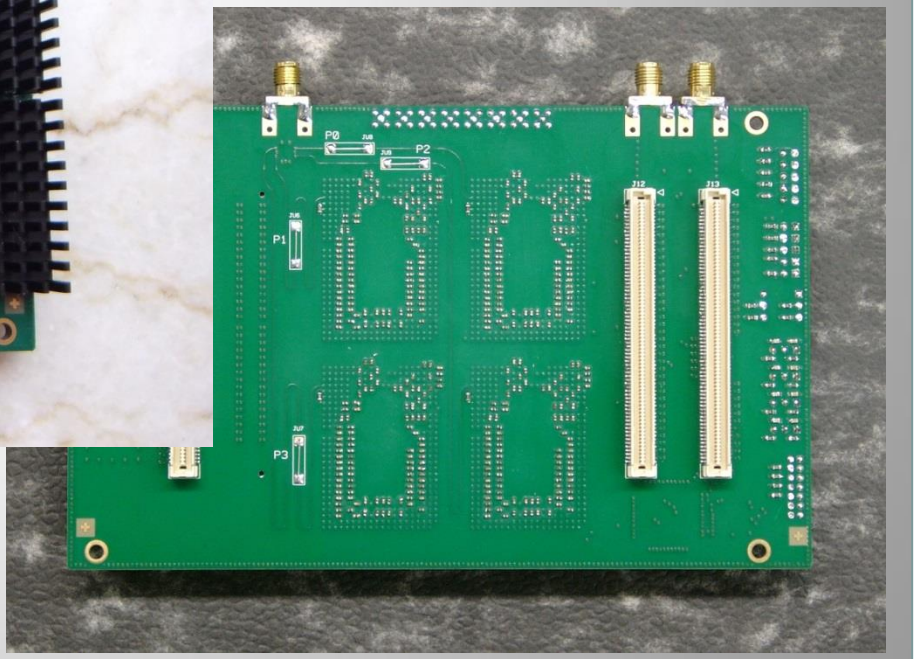
Geodesy

- **VGOS ultra-wide-band VLBI system**

ADB3L

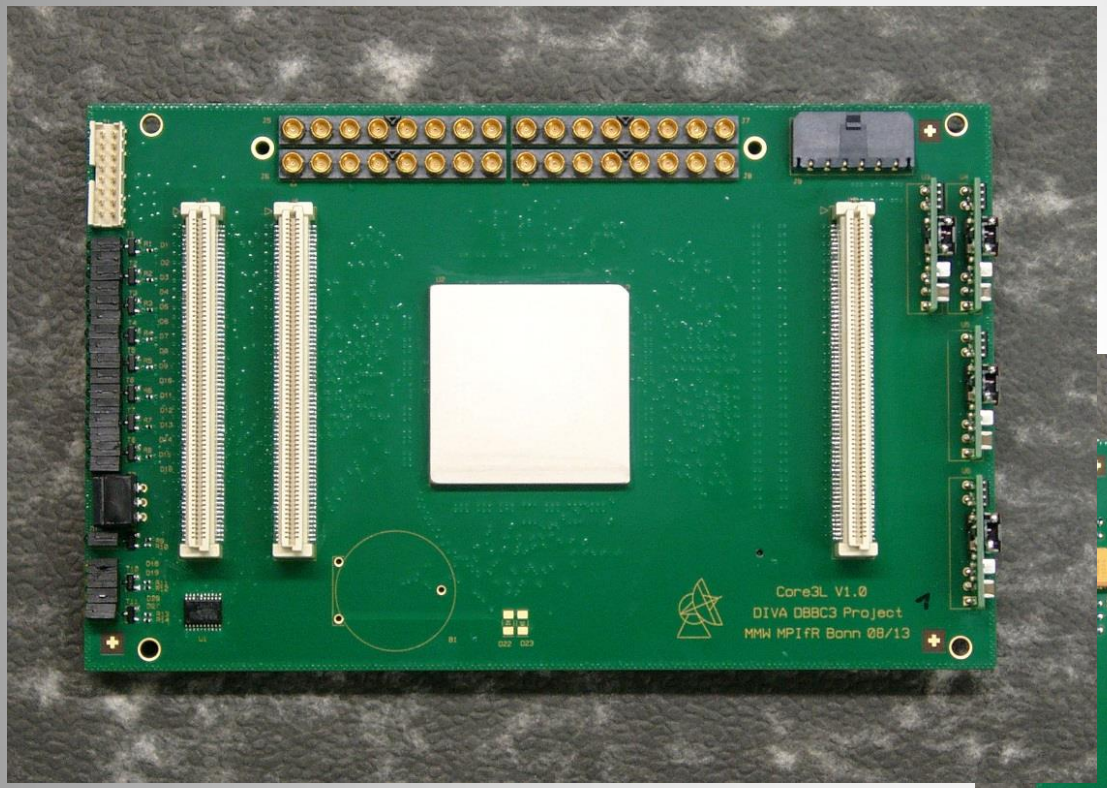
- Number of IFs: **1 - 4**
- Equivalent Sample Rate IF: **8 GSps**
- Instantaneous bandwidth: **4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC

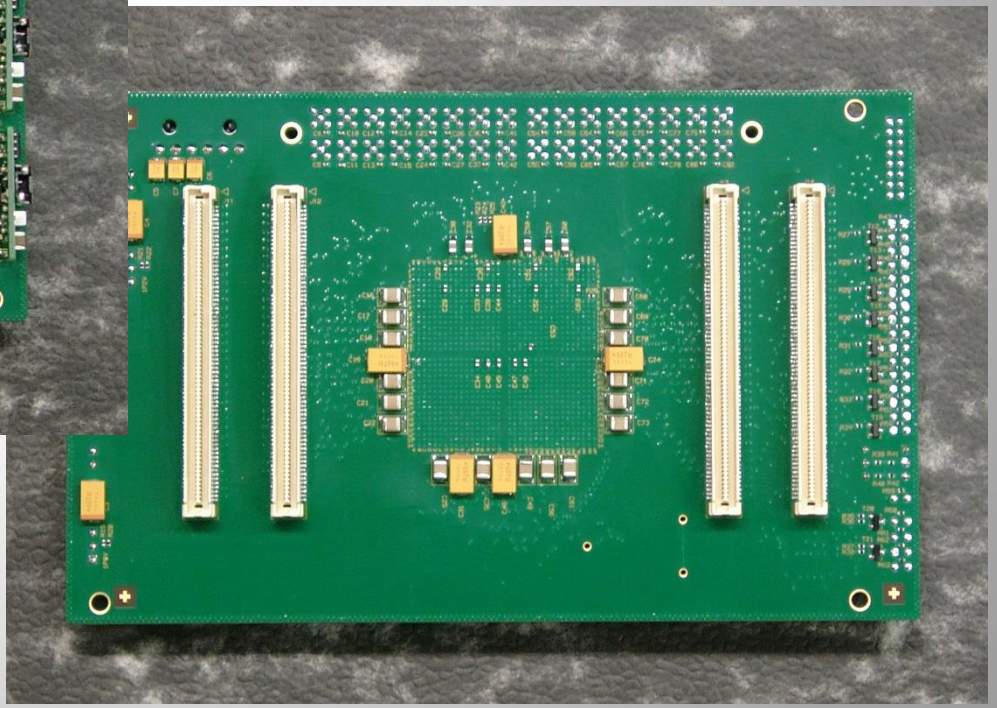




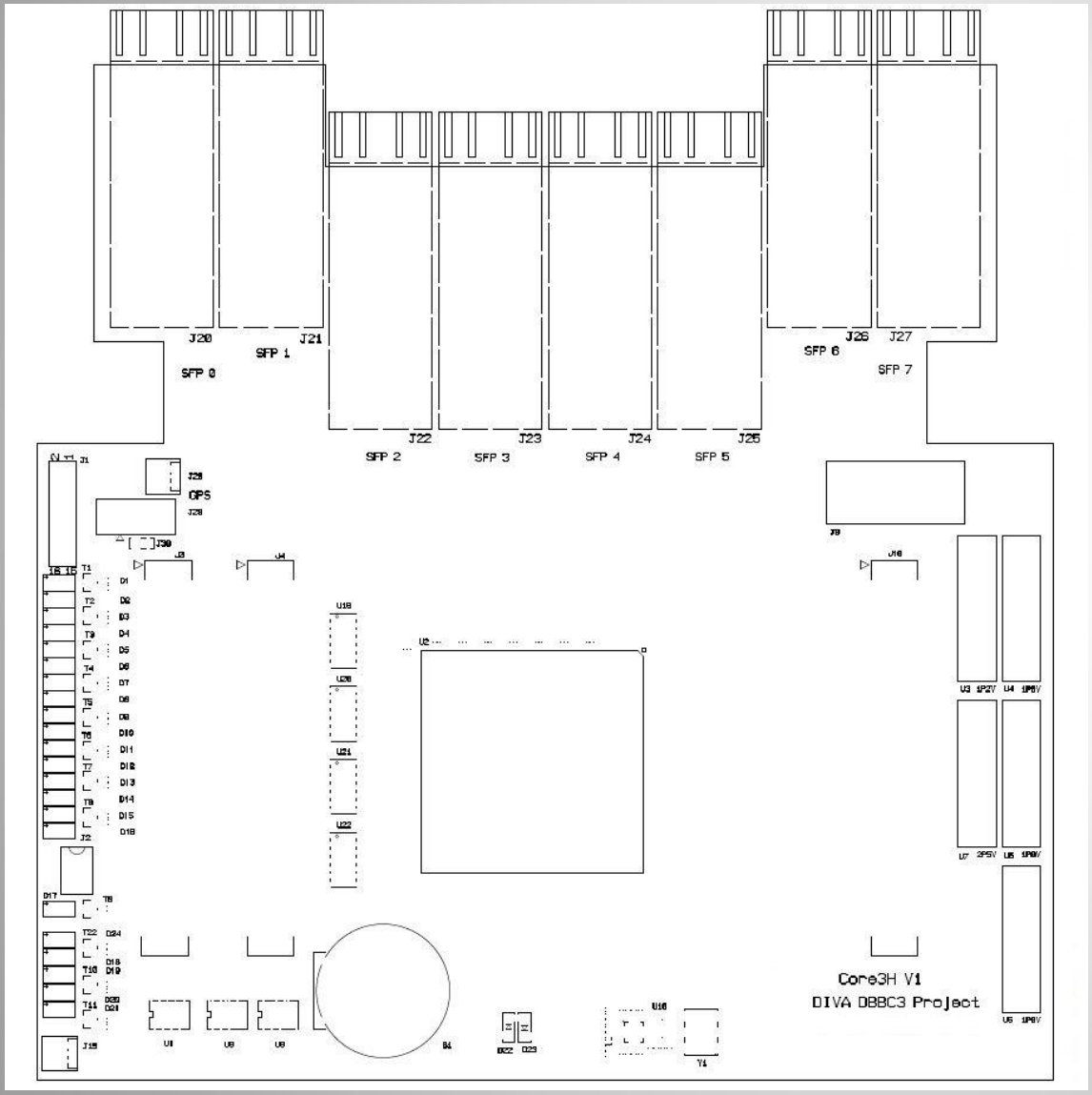
CORE3L

- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : **1 x 4GHz, 2 x 2GHz, 4 x 1GHz**
- Processing capability: **DDC, PFB, DCS**
- Output bus: **HSO**
- Output bus mode: **DDR VSI-H**
- Inter-board bus: **4 Input + 4 output Cu 10GE**
- Compatibility with existing DBBC environment



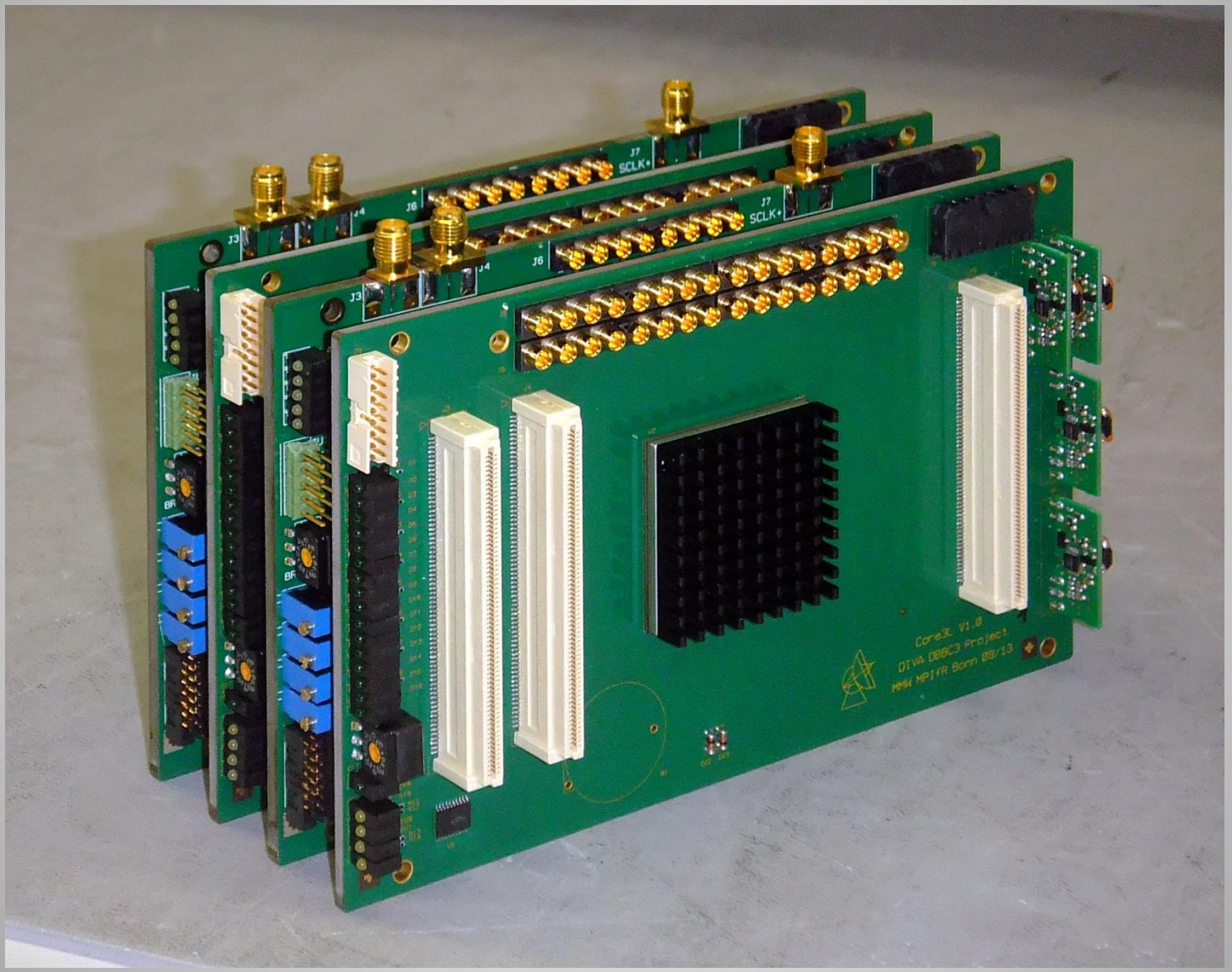


CORE3H

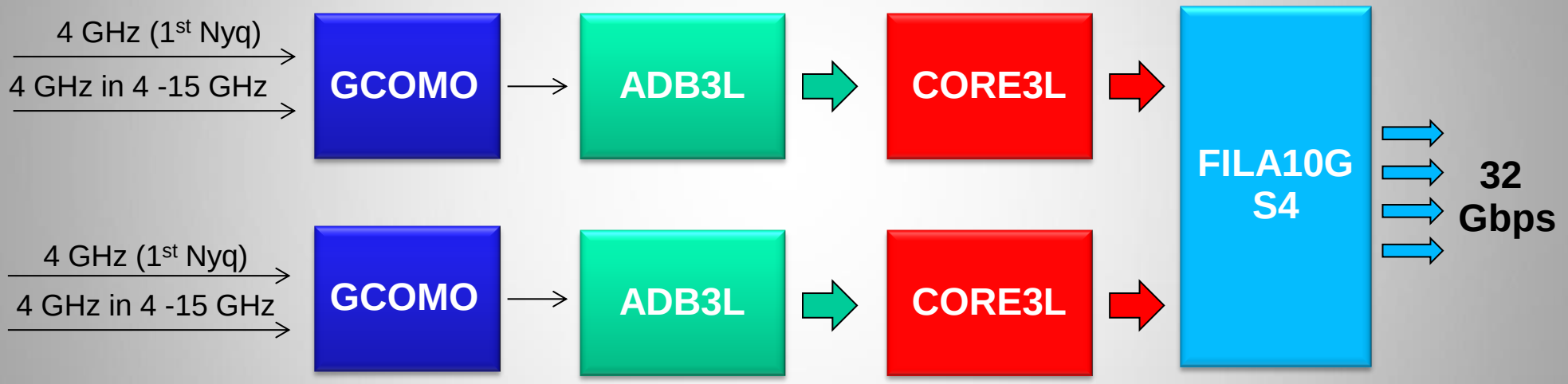


- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : 1 x **4GHz, 2 x 2GHz, 4 x 1GHz**
- Processing capability: **DDC, PFB, DCS**
- Output: **8 x 10GE SFP+**
- Inter-board bus: **8 Input 10GE SFP+**
- Compatibility with existing DBBC environment

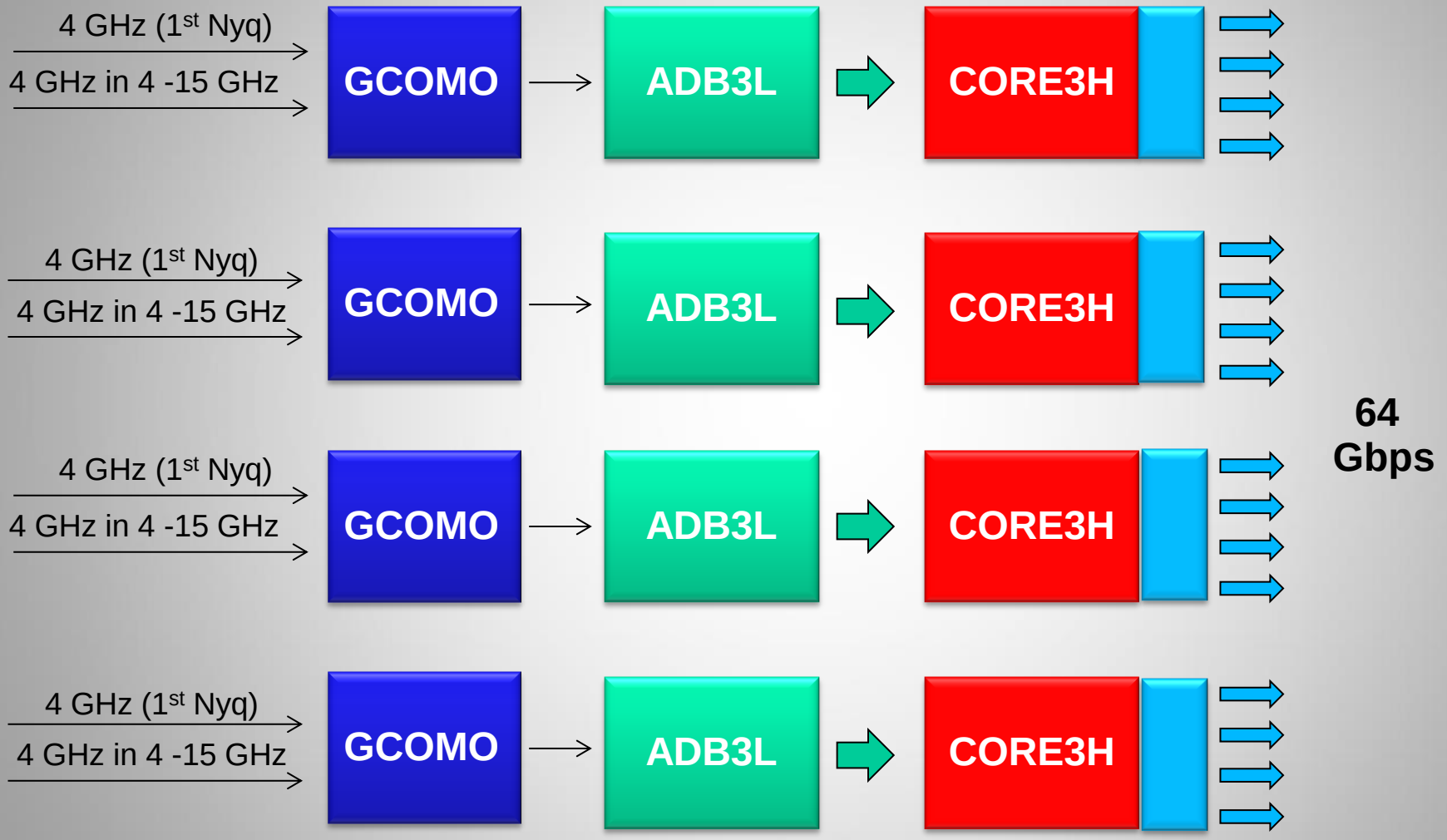
Stack with 2 ADB3L and 2 CORE3L
4 GHz bwd dual polarization



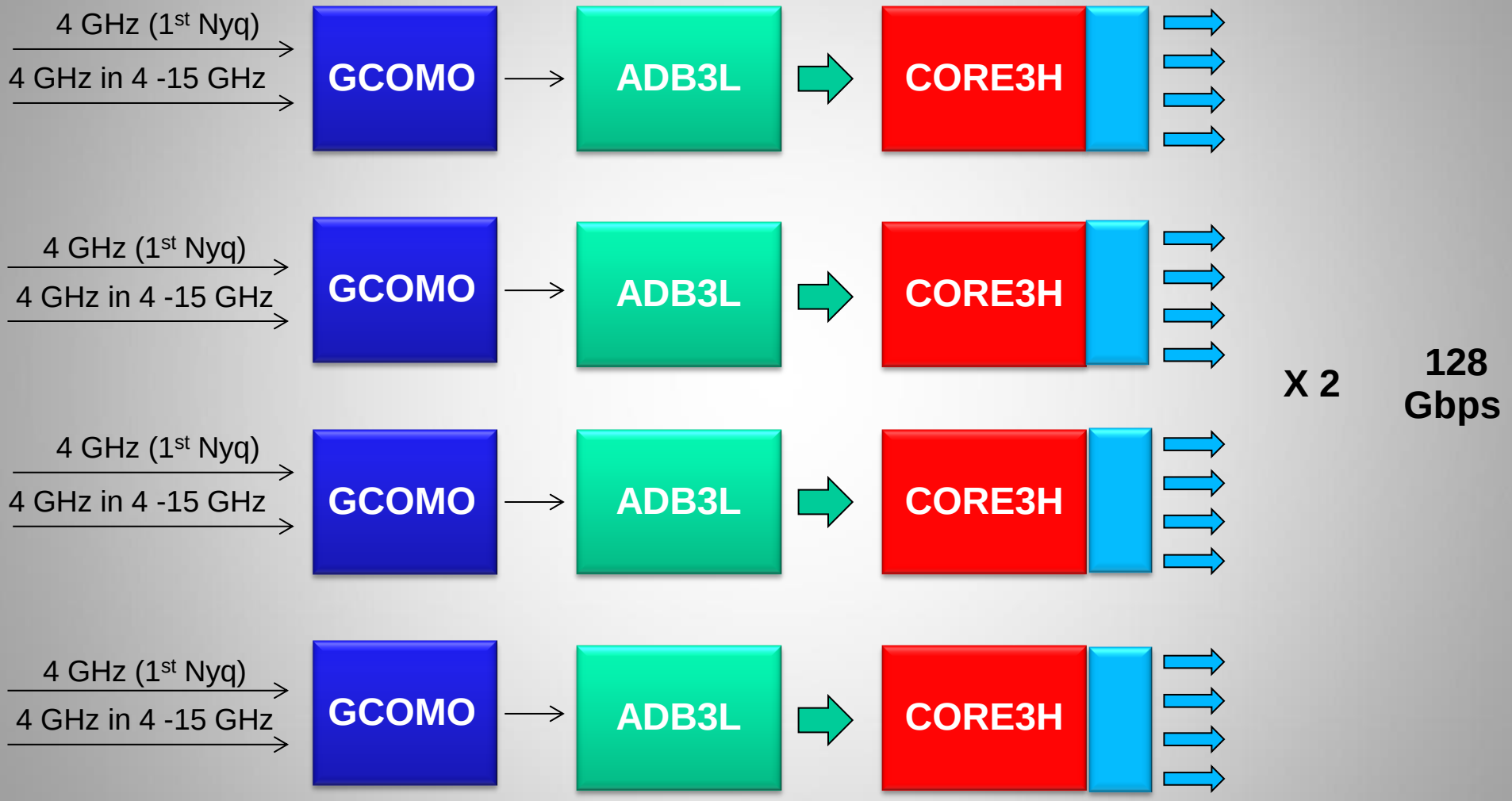
DBBC3L-2L2L Architecture



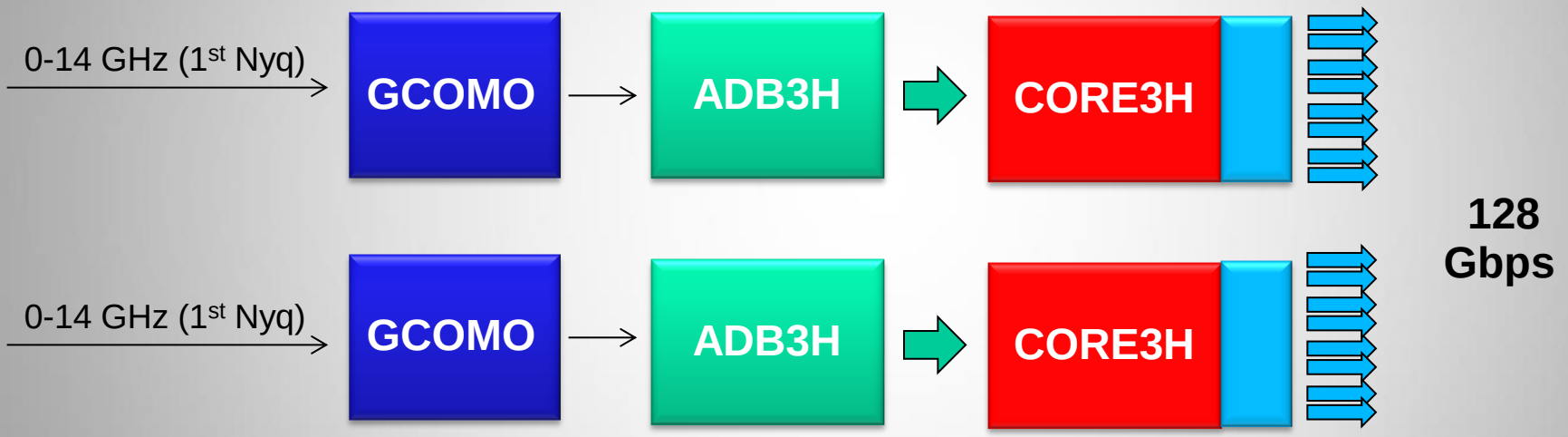
DBBC3L-4L4H Architecture



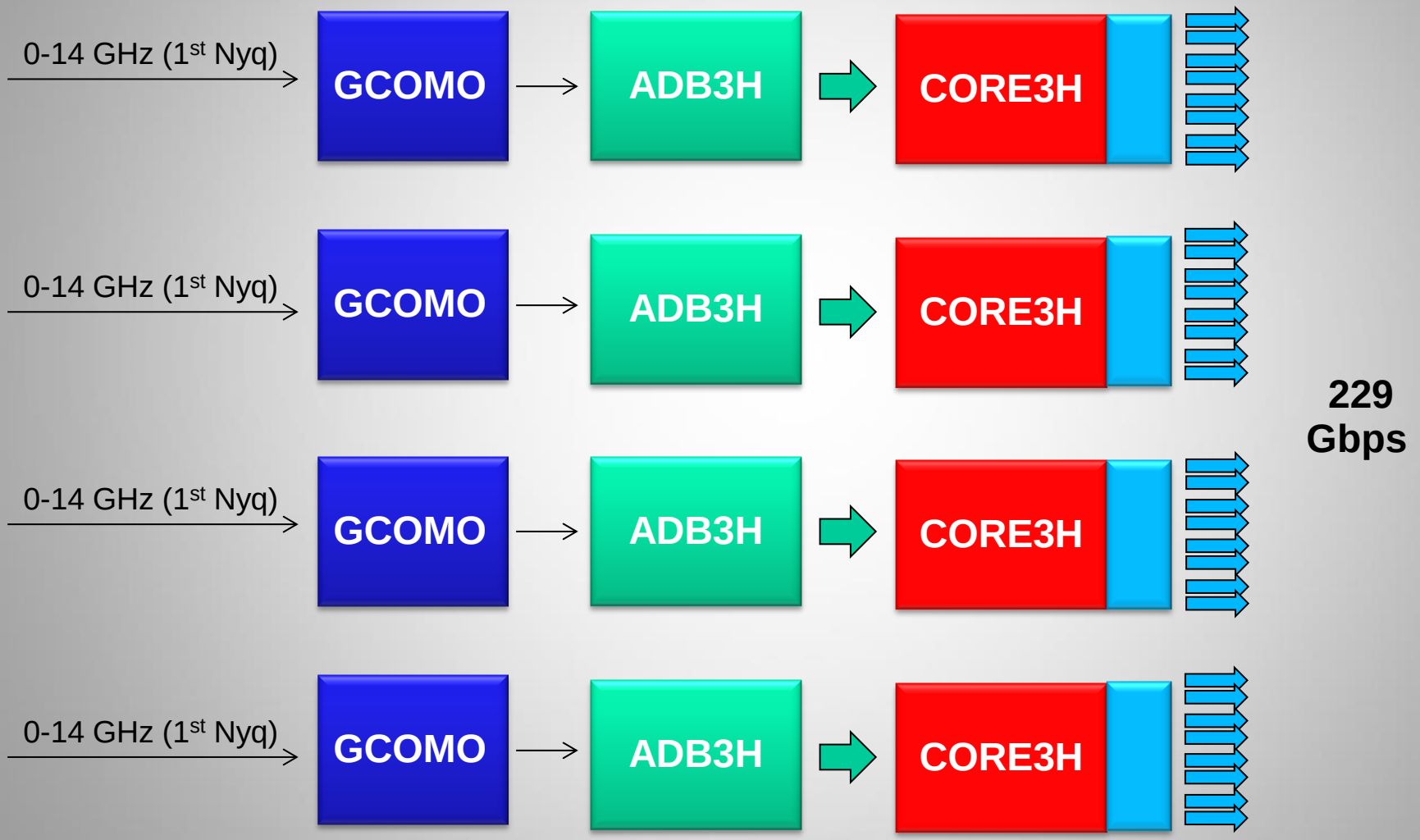
DBBC3L-8L8H Architecture



DBBC3H-2H2H Architecture



DBBC3H-4H4H Architecture



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NETWORK
HAT Lab

DBBC3L -2L2L

DBBC (Digital Base Band Converter) family overview:

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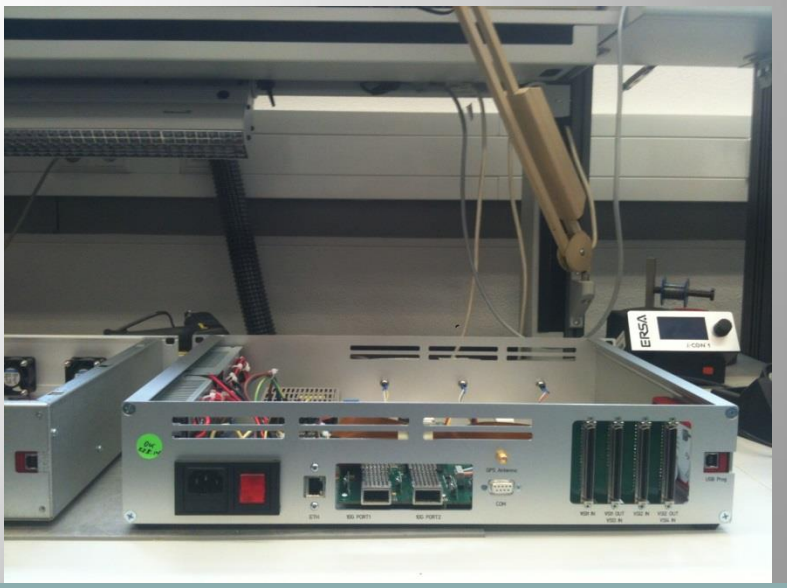
- VLBI network shifters ←
- VLBI data buffers
- VLBI digital receivers
- VLBI synthesis arrays

FILA10G

Shifts VLBI data on Internet – 16 Gbps

4 x VSI-H <> 2 x 10GE

- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode support an independent block of destination addresses
- Decimation and bit-mask selectable



FILA10G-S4

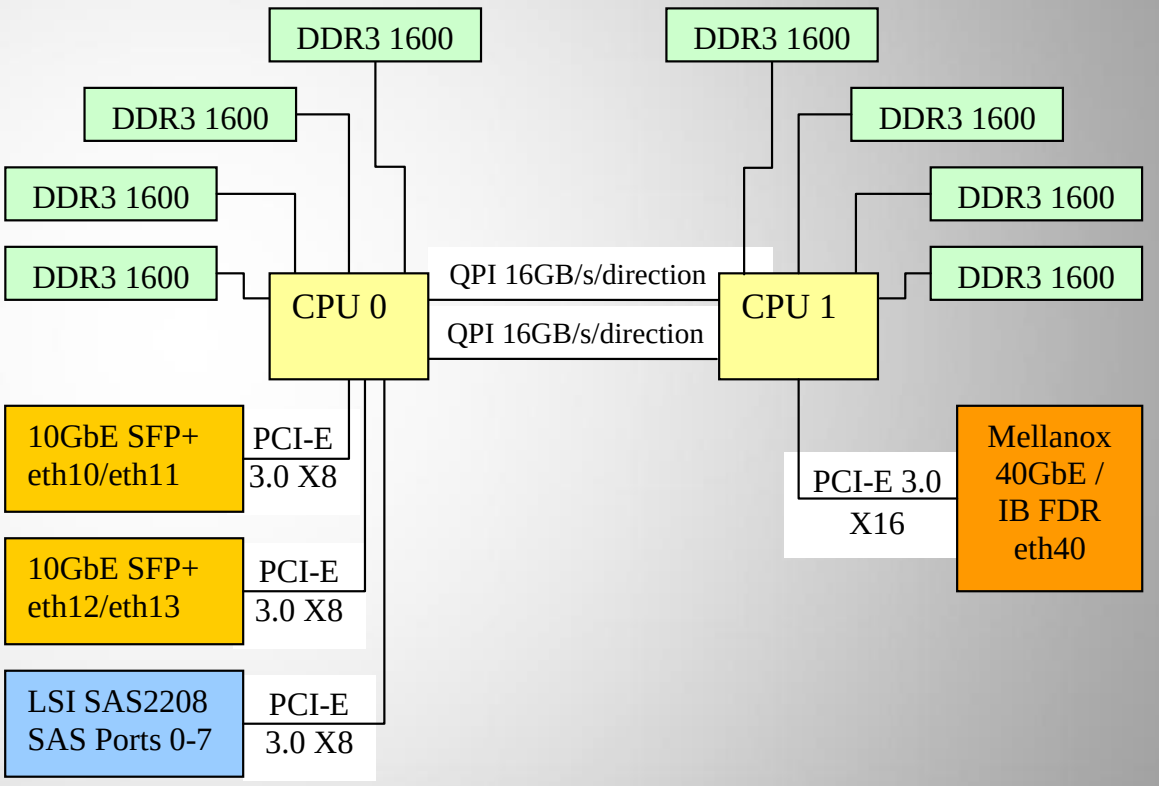
Shifts VLBI data on Internet – 32 Gbps

8 x VSI-H <> 4 x 10GE

- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode support an independent block of destination addresses
- Decimation and bit-mask selectable

FILA40G Architecture for 32 Gbps

- 2 x Intel Xeon E5-2670
  - 8 core 2.60 GHz
- 8 x 8GB DDR3 1600
- 8 Onboard SAS2 ports
- 4 free PCI 3.0 x8 slots
  - To be used to add extra SAS2/3 ports



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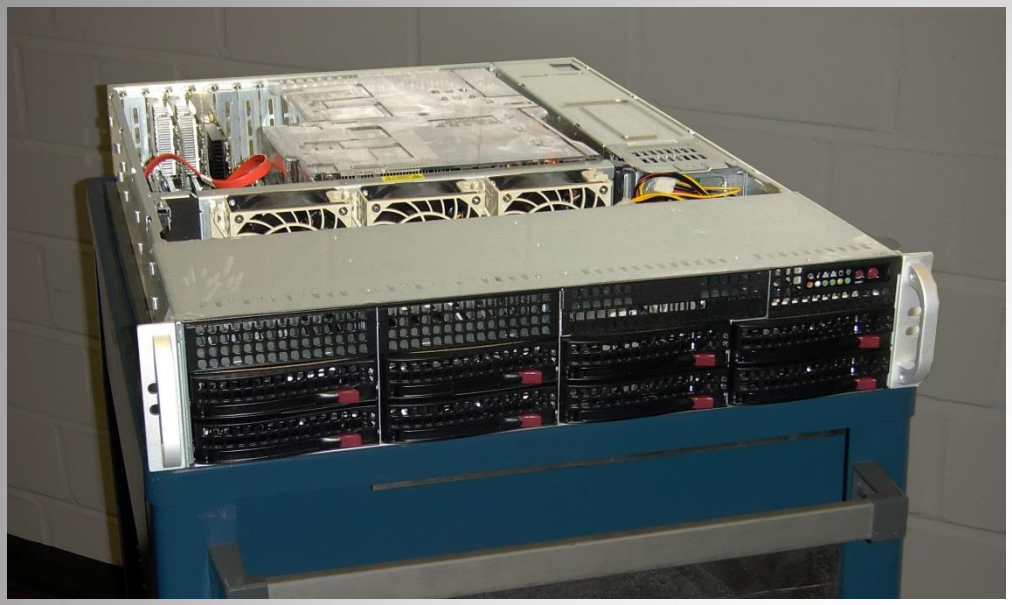
FILA40G General Key features

- 4 x 10GE Inputs / module
- 1 x 40GE Output / module
- Optional disk storage
  - Expected to record at 32Gbps sustained / module
  - Compatibilty with Mark6 disk packs/chassis being investigated
- Stream aggregation
- Format conversion/VDIF threading
- Packet filtering
- Pulsar gating
- Timekeeping via NTP and/or GPS module
  - Propagates UTC to other connected devices via DBBC Local Network (DLN)

FILA40G



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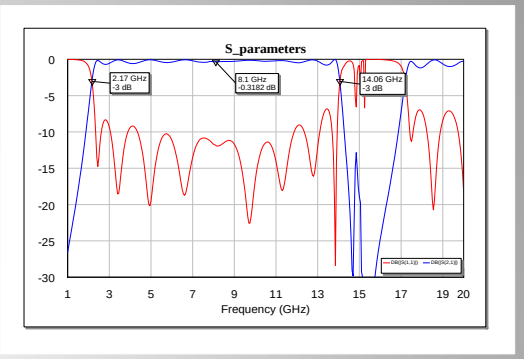
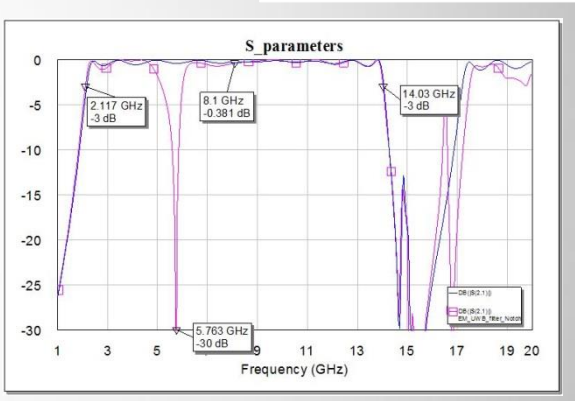
DBB*R* Receiver Front-end

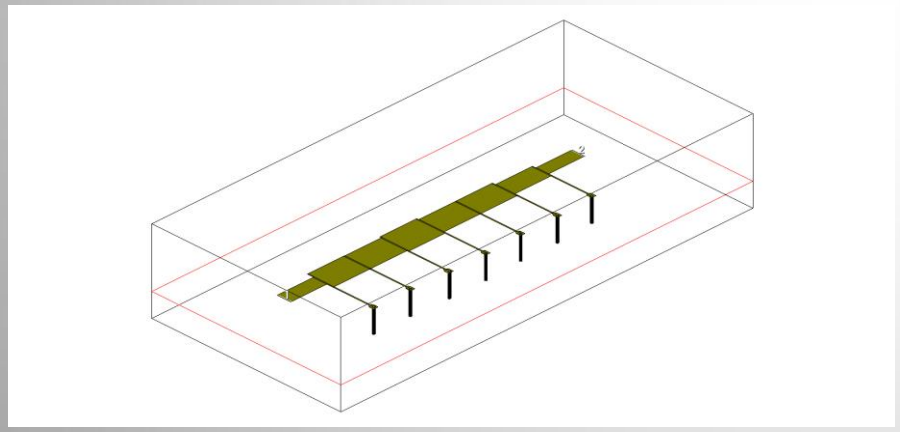
- Feed from an original project for telecommunication, deeply modified
- Dual linear polarization, 1 Caltech LNA / polarization
- Circular polarization generated in the analogue domain
- Full range 1 – 14 GHz
- Radiation pattern vs frequency optimized for 3-14 GHz:
- Antenna factor vs frequency optimized for 3-14 GHz
- Entirely in copper optimized for cryogenic use
- Custom cryogenic filters integration in the antenna body
- Full band level adaptation for the digital part (ADB3H)

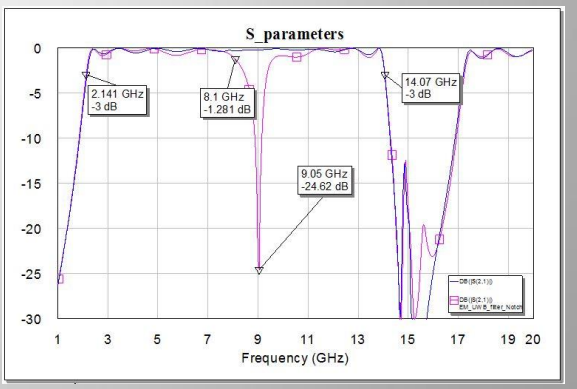
Ultra Wide-Band HTS filter

- High temperature superconductor microstrip technology
- Response bandwidth from 2.2 to 14 GHz
- Low in-band insertion loss
- High out-of-band insertion loss
- In-band maximally flat group delay
- Small overall dimensions









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DBBC3: AntArr Synthesis Array

Fig. 1 DBBC3L

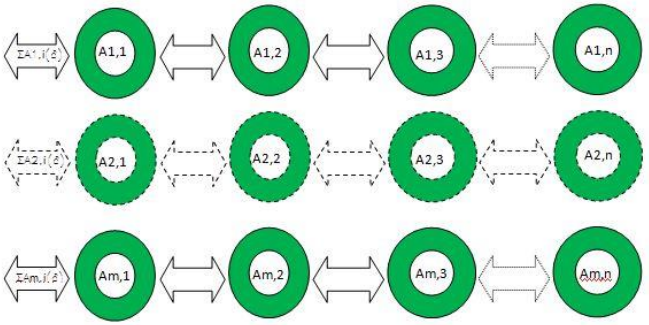

Fig. 2 Antenna Array

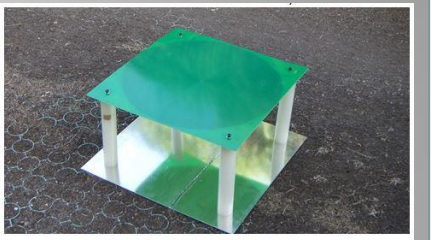
Fig. 3 10—1000 MHz Antenna prototype

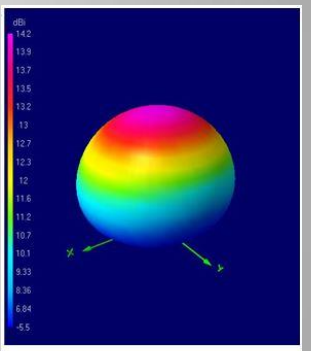

Fig. 4 Single antenna prototype 3D

ARRAY GENERAL FEATURES AND BEAM SYNTHESYS

- Antenna Prototype frequency range: *10—1000 MHz*
- Max. number of antennas in a single arm: *32*
- Max. number of arms in a single DBBC3L: *32*
- *Max. observation bandwidth at each arm: 128 MHz*
- *Analogue delay compensation digitally controlled at every antenna*
- *Analogue summation for each arm at every antenna*
- *Digital correlation between any element of the array*
- *Digital correlation between any element of the array and the synthesized beam*

STATIONS

Two stations have been equipped for testing the network capability: one in the Noto radiotelescope area, the other on the northern slope at low altitude (600 mt.) of the Etna volcano.

Fig. 5 Noto-Etna baseline, 114 Km

Fig. 6 Antenna prototypes in Noto

Fig. 7 Drone equipped with transmitter 327-654-981 MHz