IAA Correlator Center

Valery Gratchev

Abstract

In 2003 the IAA S2 correlator TISS-1M processed six sessions for radio source structure investigation. Also, some revisions and updates were made for control and post processing programs. The Institute of Applied Astronomy is developing Altera FPGA-based scalable correlator PARSEC with Mark4 specification. We have developed the prototype correlator MicroPARSEC. PCI-bus correlator board MicroPARSEC has standard office PC board format.

1. General Information

The S2/Mark3 correlator (Figure 1), new correlator MicroPARSEC and PARSEC are located at and staffed by the Institute of Applied Astronomy in Saint-Petersburg, Russia. The correlators are sponsored and funded by the Russian Academy of Sciences, by the Russian Foundations of Basic Research and by the Russian Ministry of Sciences and Technologies. Dedicated to processing geodetic, astrometric and astrophysical VLBI observations, the general role of the correlators is as an operational processor for VLBI observation in Russia.

Figure 1. **S2 correlator TISS-1M at the IAA correlator center in Saint-Petersburg.**

There are three racks with S2-PT terminals at the center of the back plane and six racks for

correlator devices on the left and right from play back terminals. On the right of front plane, there is a table with control computer with correlation software and post processing program PrOut.

2. Correlation Processing

In 2003, we processed the following S/X experiments at Svetloe-Zelenchukskaja baseline for radio source mapping by using of amplitude method.

04-06 February and 28 February 2003,
04-05 March 08-16 March 2003,
20-28 April 2003, 22-25 May 2003,
09-12 August 2003,
14-17 September 2003.

Also, we made some fringe tests to investigate the antenna pointing accuracy at Svetloe and Zelenchukskaija.

3. New Correlators

The Institute of Applied Astronomy is developing Altera FPGA-based scalable correlator PARSEC with Mark4 specification. The correlator unit uses PCI-bus correlator boards, standard CompactPCI hardware with single board Intel Pentium control computer and standard Linux operating system (Figure 2). We have estimated that it is possible to provide 4-station and 16-channel 1- or 2-bit data processing by using single correlator unit with Mark5 VSI compatible playback system for VLBI and e-VLBI.

We have developed the prototype correlator MicroPARSEC. PCI-bus correlator board MicroPARSEC (Figure 3) has the following features: standard office PC board format, single board supports 2 cross-correlation channel for one baseline, operation at input data rate to 64 Msamples/sec/channel, 1 or 2 bit sampling, integrated input data rate to 512 Mbit/s, the board can be connected directly to Canadian S2-RT or S2-PT.

The features of the IAA correlators are summarized in Table 1.

We have produced and tested four MicroPARSEC correlator boards, which also may be used as scalable spectrum analyzer for station phase cal extraction and other different system diagnostic and/or spectral line real time observation data processing in single dish mode on our radio telescopes in Svetloe, Zelenchukskaya and Badary. We are going to start volume production in order of the correlator board MicroPARSEC for standard office PC with standard Windows 98/2000/XP operating system and special control and monitor program developed in IAA.

4. Updating the Control and Post Processing Programs

One of the major updates was made to the control correlator program for serial processing data of geodetic S2 VLBI observation at Russian stations. The program is installed in IBM PC Pentium III under Windows 98. For the calculation of model for delay tracking and fringe stopping the program package ERA developed at the IAA is used.

The post processing program PrOut was updated to extract the observables from serial raw correlator output data. The PrOut in Visual C++ v.6.0 is installed on IBM PC Pentium IV computer under Windows XP operating system.

Table 1. Comparison of the correlators at the IAA

	TISS-1M	**MicroPARSEC**	**PARSEC**
Year of production	1993	2003	2004
Data input format	Mark3	S2/VSI	S2/VSI
Number of channels	30	2	16
Number of lags	8	64	64
Processing rate/ch	4 Mbps	64 Mbps	64 Mbps
Sample bit	1 bit	1 or 2 bit	1 or 2 bit
Phase resolution in fringe rotation	32 bit	32 bir	32 bit
Phase cal detect	1 Hz ÷ 1 MHz	1 Hz ÷ 4 MHz	1 Hz ÷ 4 MHz
Accumulation counter	24 it	30 bit	30 bit
Parameter period	5ms ÷ 1s	50ms ÷ 50s	50ms ÷ 50s
Pulsar gate	No	Yes	Yes
Main logic	Standard logic 1C	FPGA	FPGA
Data transfer	S2	S2/Mark5B	S2/Mark5B
Baselines	3	1	6

Figure 2. **The prototype of Altera FPGA-based scalable correlator PARSEC with Mark4 specification.**

5. Conclusion/Outlook

Full construction of PARSEC correlator will be a major effort in 2004. The development, integration and expansion of Mark5 VSI compatible units will also be a priority.

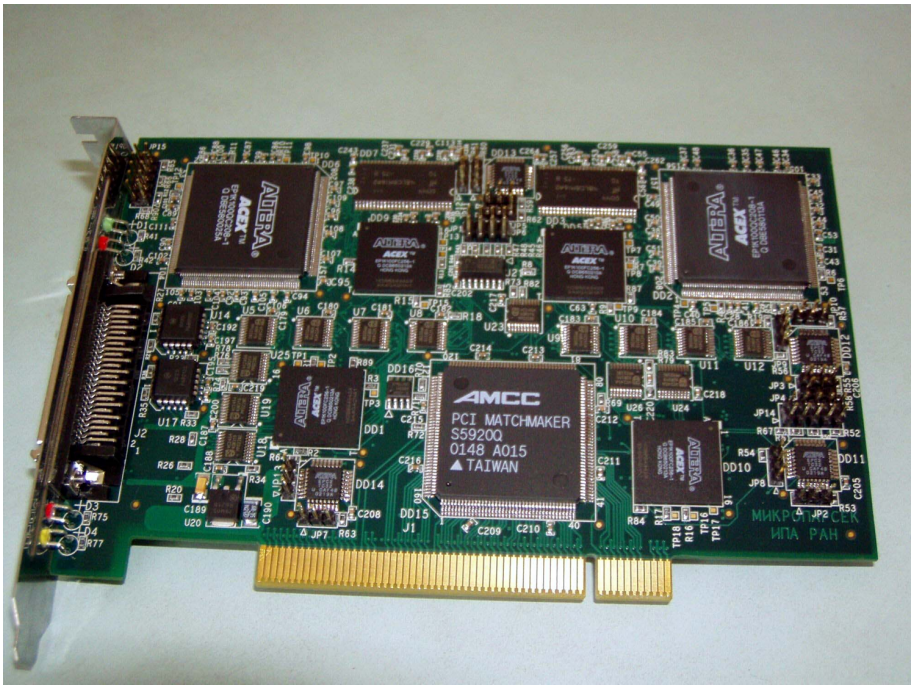

Figure 3. **PCI-bus correlator board MicroPARSEC.**