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Abstract The experience of operating the fast slewing, new radio telescope RT-13 showed that domestic VLBI observations for extreme characteristics are not enough. It is necessary to carry out regular observations as part of the international VLBI network, most of whose radio telescopes use only the narrowband backend system. To ensure compatibility, the RT-13 backend system was expanded to have the external digital converter bank (DDCB).

1 External Digital Downconverter Bank for BRAS

1.1 Introduction

Broadband Acquisition Systems (BRAS) have been used on new, fast slewing radio telescopes RT-13 of the "Quasar-KVO" complex from 2014 [1]. The system implements eight wideband channels of 512 MHz that allow the achievement of high sensitivity of the radio interferometer but complicate the processing of joint observations with narrowband types of backends which are still used on most existing VLBI radio telescopes. To simplify such observations, IAA RAS is developing an external digital downconverter bank (DDCB) [2]. The results of the development are presented.

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1.2 System Structure

Three BRAS outputs are connected to the DDCB in parallel with the data transferring and recording system (DTRS) through the high-speed Cisco Nexus switch (Figure 1). Three channels are required to simultaneously receive data of two X-bands and one S-band from the BRAS outputs. This provides a regular geodetic observation mode with frequency synthesis in 270 MHz at S-band and 720 MHz at X-band respectively.

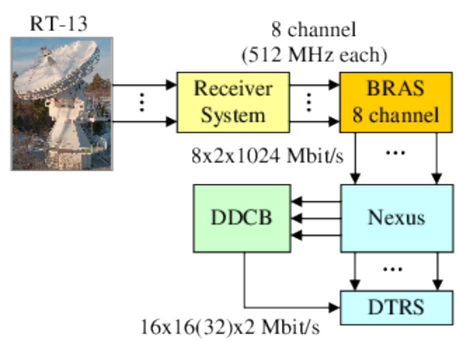

Fig. 1 The connecting structure for DDCB to RT-13.

The DDCB includes three optical receivers that provide the physical layer for transmitting and receiving the data flows through 10 Gbit/s Ethernet fiber-optic lines, a digital signal conversion module that is implemented in the field programmable logic gate array (FPGA), an Ethernet interface controller, and two local reference oscillators.

The FPGA performs the following operations: buffering data, transforming specified spectrum areas to video frequency, formation of output data, and containing 16 narrowband channels in VDIF format [3]. Output data from an FPGA GTX port through the optical transceiver SFP + are transmitted to the data buffer device by a 10 GE Interface.

The DDCB is controlled by a radio telescope central computer via 10/100/1000 Ethernet interfaces. A MicroBlaze processor for control is implemented in the FPGA configuration.

The digital converter module is realized on a KC705 development board from Xilinx (Figure 2) with an XC7325T FPGA. The digital converter module contains three independent data buffers, the three pre-filters based on a polyphase filter bank [4], a 16-channel switch, and 16 digital frequency converters. The processing of digital flows in each downconverter is divided into several stages: separation of the upper and lower sideband signal after a pre-filtration stage, moving a predetermined portion of the spectrum to lower frequencies, video bandwidth formation, and subsequent formation of two-bit data flow. In addition, the FPGA configuration contains a timer, a VDIF frame data pack unit, an Ethernet frame pack unit, a data capture module, and a MicroBlaze control processor.

Fig. 2 The DDCB with an open case.

The output formatter of the VDIF-frame integrates the data from downconverter outputs into one total flow, which is then broken up into packets of a given size. The frame headers include service information obtained by decoding the input data from BRAS, as well as additional DDCB parameters. These data observations, together with service information packed in raw Ethernet-packets with the possible addition of UDP and IP headers, is transmitted through the interface to the transceiver 10 GE receiver-transmitter and next to the data buffering device on the radio telescope.

1.3 The Software

The controller was made on the basis of the MicroBlaze processor, which, formed in the FPGA, is the main element of the DDCB management system. Upon receiving a request, obtained via Ethernet, the controller forms a response, which contains control information (e.g., a synchronization check, the presence of transceivers, and other information). The obtained data are used to control the system operation.

To communicate with a computer through a UDP FPGA, an Ethernet-controller PHY 88E1111 and GMII interface is used. Text commands of UDP-packets from the control computer are processed by the MicroBlaze processor, which was formed in the FPGA.

1.4 Conclusion

The main DDCB components were developed and debugged: data buffer, pre-filtering, sideband separator and digital down converter, and output signal quantizer. The final adjustment of the developed firmware is being carried out to optimize FPGA resource utilization. Laboratory tests of the DDCB are currently being performed, and the first test with real observations has to be scheduled to be performed until mid-2017.

References

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