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Parallel Data Processing System

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Abstract

Signal processing in the current correlation processing algorithm is bit-serial. The speed of correlation is limited by the speed of the correlation device, and, as a result, the device speed limits observing bandwidth. The algorithm is thus not effective for astronomical applications. To overcome this problem, I have developed a new correlation-processing algorithm for parallel data. We focus on the derivation of serial data-processing algorithms for parallel data.

1. The Current Parallel-data Processing System

The improvement of sampling and recording technologies to achieve higher speeds of data processing is required. The data-processing speed, however, is restricted by the correlation device-clock in serial data processing. In recent technologies, we can obtain the data rate to several giga-bits per second. New 1024-Mbps recorders including GBR-1000, Mark-IV, S3, and DIR-2000U, will become available.

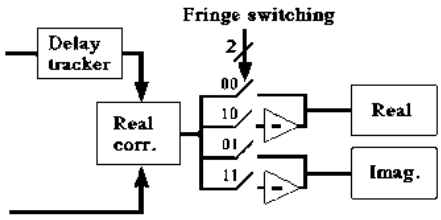


Figure 1. Block diagram of a current giga-bit correlation system GICO.

The GICO (giga-bit correlator) is the first parallel data processing system. GICO's correlation processing algorithm operates on parallel data (Fig. 1). However, because fringe stopping is carried out in parallel data steps rather than in bit steps, there is some loss of coherence. The continuous delay tracking range is limited to 8064 bits.

2. New Parallel Data Processing System

When designing a correlation processor, we must take into account delay tracking, fringe stopping, and 90-degree phase jumps. We focus on how to derive processing serial data algorithms for parallel unit of data. The serial data processing algorithm of the Mark III is sophisticated, so I wished to convert it to operate on unit of parallel data.

2.1. Delay Tracking Based on Parallel Data

We consider the operation of the parallel delay tracking algorithm in one-bit steps. We assume that there are n parallel data bits. The circuit consists of parallel shift registers A and B (Fig. 2).

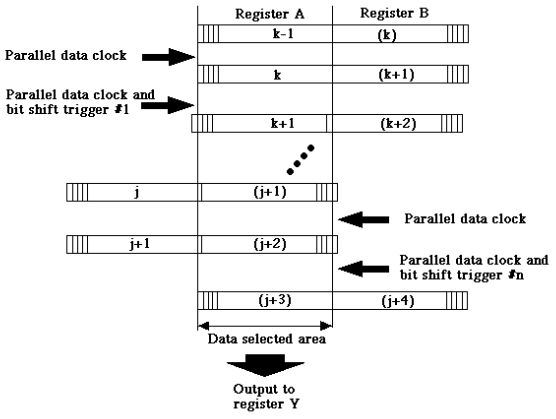
Initially, the $(k-1^{th})$ datum is loaded into parallel shift register B from the parallel data buffers for Station-Y data; these buffer memories work in a pipeline sequence.

The k^{th} data bit is then loaded into parallel shift register B from the buffer memory. At the time at which the data in shift register B are shifted to shift register A. The data output to register Y for correlation with Station X data, displayed as the data selected area between two lines in the figure, is selected by a parallel data selector which is controlled by a control counter. When a bit shift occurs, the control counter is incremented/decremented. All of the circuits are driven by a parallel data clock. The shifting of bits is thus performed with this parallel data clock's timing.

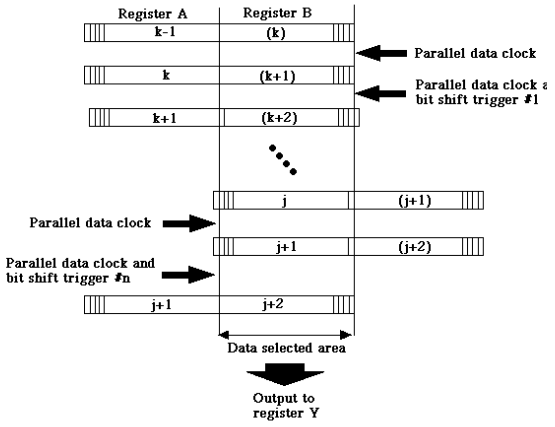
Next, we consider the timing of bit shifts in more detail. We can detect a bit shift in the following way. We performed *a priori* calculations of the Earth's rotational parameters including wobble, diurnal polar motion, diurnal rotation, nutation, precession, aberration, time difference, etc.. τ_g was calculated and approximated as a fourth-order polynomial in the built-in controller which was adopted from the KSP correlator [1]. Comparing the delay of the current parallel clock cycle with that of the previous cycle, we find that the difference in time is n (parallel number) of the sampling period when the delay difference is more than 1 bit, fractional delay in the parallel bits was occurred. Usually, the values of all bits of the bit-select control register are "0". If there is a fractional delay in the parallel bits, "0" and "1" are sent to the bit-select control register. The fractional bit shift timing is indicated by the boundary between the "0" and "1" bits (Fig. 3). Parallel data can be bit-shifted in one-bit steps.

When the control counter's value reaches its maximum (left-hand side: Fig. 2), the next data bit is loaded into the parallel shift registers from the parallel data buffers and the conditions of registers are simultaneously set to "zero" on the next data-clock cycle.

When the control counter reaches zero (right-hand side: Fig. 2), the next data bit is unloaded into the parallel shift registers from the parallel data buffer, and the conditions of the registers are simultaneously set to "full" on the next data-clock cycle.



Memory control sequence (positive delay rate). Data numbers in brackets are loaded data from buffer memory.

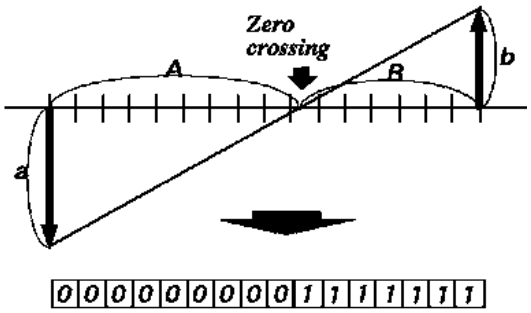


Memory control sequence (negative delay rate). Data numbers in brackets are loaded data from buffer memory.

Figure 2. Delay tracking.

2.2. Parallel Fringe Rotation

We performed *a priori* calculations in the built-in controller for every cycle of the parallel data clock.



Usually, the bits of the phase control register are all "0". Comparing the fringe phases at time k with those at time (k+1), we find that the difference in time is n (parallel width) sampling periods when the phase difference is more than $\pi/8$, and "0" and "1" are set in the phase control register. The boundary between "0" and "1" bit indicates the fractional bit shift timing, and the fringe phase must be changed by $\pm\pi/8$ radian. The position of the boundary is determined (Fig. 3) by the division circuits.

Figure 3. Zero cross decision.

2.3. Parallel 90-degree Phase Jump

Fringe stopping is performed on the band center frequency; a 90-degree phase jump and a bit shift are done simultaneously. The bit select control register (for delay tracking based on the parallel data but in one-bit steps) also controls the 90-degree phase jump. The timing of the 90-degree phase jump is indicated by the boundary between the "0" and "1" bits of the bit select control register (Fig. 3).

2.4. Data Synchronization

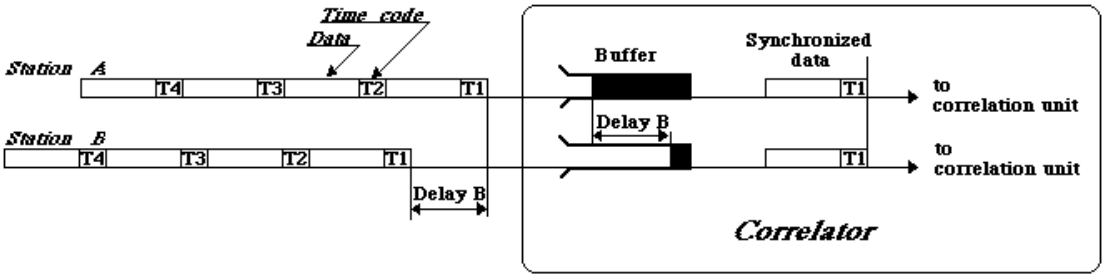


Figure 4. Data synchronization sequence in case of real-time VLBI.

In real-time correlation [1], the correlator is equipped with a function for automatic data synchronization so there is no need for external units. Time stamps composed of indicators of year, day, hour, minute, second, and the SYNC code used in time code recognition are inserted

in the data at regular intervals. To absorb the transmission path delay, signals are stored in the buffer memory at the same time as the time stamp is received. This time stamp is generated by the ATM interface unit. Readout starts immediately after the time stamps from all observation stations have arrived, and this allows synchronization of timing. The data are only output to the correlation part after the timing has been synchronized, so the output data for each station are correct up to the time at which the time stamp is applied. The size of the buffer memory is 64 Mbits/ch. The same data synchronization function is used in tape-based correlation.

3. System Evaluation

The giga-bit system consists of a giga-bit sampler, an ATM interface unit, and a giga-bit correlator.

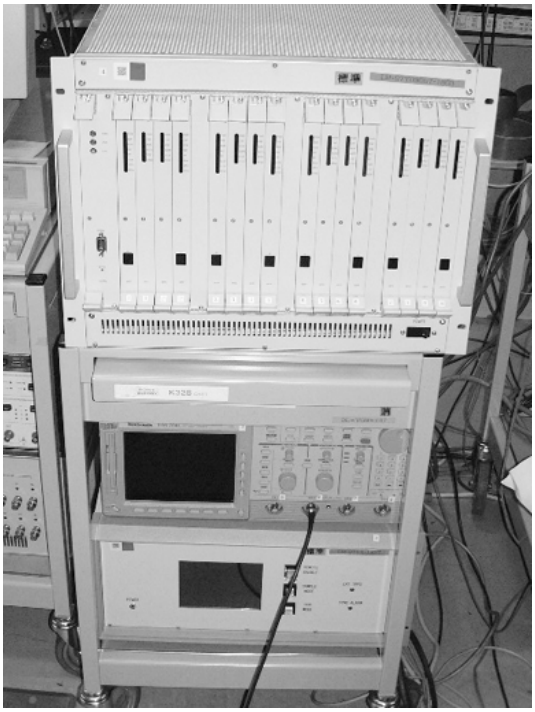


Figure 5. Picture of giga-bit system (Upper: giga-bit correlator, middle: sampler (TDS-784), lower: ATM interface).

The giga-bit sampler is based on a commercially available digital oscilloscope (Tektronix TDS784). The development of this radio astronomical A/D sampler began in 1995. The oscilloscope has four analog-to-digital sampler chips, each of which operates at a maximum speed of 1 Gbps with a quantization level of eight bits for each sample. The two MSBs quantized bits of each sample (ch.) are extracted from the digital oscilloscope and sent connected to the ATM-interface unit. The sampling rate was increased by 25.6/25, to make the original 1-Gsps sampler operated as a 1.024-Gsps sampler. This modification was applied in the A/D sampled signal pick-up daughter board in the oscilloscope. The output signal is sent via high-speed parallel coax and the (4-channel) * (256 or 512 or 1024 Msps) * (2-bit sampling) data are output from the pick-up daughter board. The oscilloscope is able to calibrate itself by signal path compensation. A self-calibration function is also used to calibrate the DC offsets of the A/D converters according to changes in the ambient temperature. This function is useful in multi-bit sampling.

The ATM interface has a real-time clock that is phase-locked to the data clock of the giga-bit sampler. The data input from the giga-bit sampler are formatted and a time code is inserted. Channel selection (1/2/4 ch) and quantization-bit selection (1 or 2 bit) are performed in the formatting section. The rate of the output of data to the recorder or ATM line is selected from among four rates, ranging from 256 to 2048 Mbps.

Fig. 5 is a photograph of the correlation system. The number of parallel data bits is 64. The

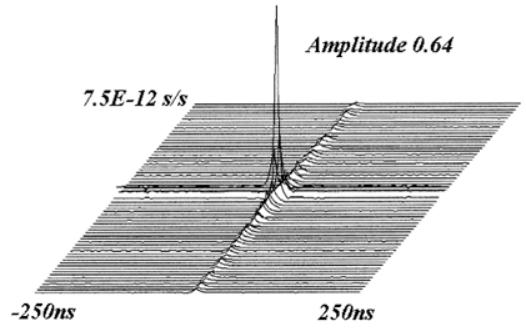
maximum speed of processing is 2048 bps/ch, and the correlator is four-channel. Each channel has 1024 complex lags.

3.1. Correlation by Using a Wavefront-clock Fringe-simulator

White noise from a noise diode is converted to simulate a signal received from a star as if it were being observed at the target station by using a wavefront clock system. If the RF noise signal is divided with one branch acquired by using a normal VLBI system and the other branch acquired by a wavefront clock system, we are able to obtain a simulation of VLBI data at two different stations, that is, a VLBI fringe data simulator. The simulator-generated virtual VLBI station data was used to check the operation of the giga-bit correlator. One set of the results of this simulation is shown in Fig. 6.

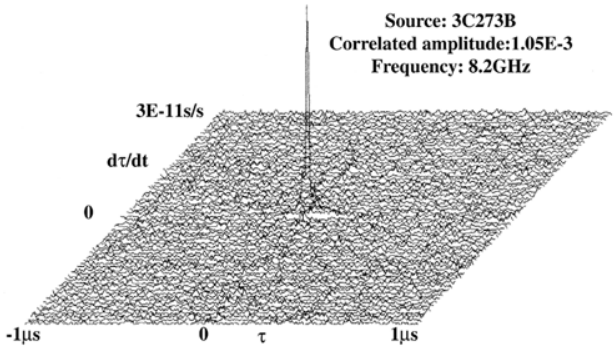
3.2. Real-time Fringe Detection using an ATM Network

A real-time experiment between the Koganei and Kashima KSP stations was carried out. The IF signal was down-converted to a wide bandwidth video signal by using a KSP local oscillator. The wide bandwidth video signal was sampled by the giga-bit sampler, and then formatted by the ATM interface unit. The formatted signal was transmitted from Kashima to Koganei via the ATM line. After that, correlation processing was performed. The experimental result is shown in Fig. 7, displayed 512 lags around the fringe. The result shows that we had been able to obtain fringes with high SNR.



Simulated result (1024 Mbps) by using a wavefront clock simulator. Correlated amplitude is 0.64.

Figure 6. System check.



Result of this system (Koganei-Kashima baseline experiment).

Figure 7. Real-time experiment.

References

[1] Kiuchi H., M. Imae, T. Kondo, M. Sekido, S. Hama, T. Hoshino, H. Uose, and T. Yamamoto, In: Real-time VLBI syatem using ATM network, IEEE Trans. Geosci. and Remote Sensing, Vol.38, No.3, pp.1290-1297, 2000.