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Low-Cost Wideband Digital Back-Ends for LOFAR⇒e-VLBI⇒SKA

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Abstract

Virtually all next-generation radio astronomy applications could be economically served by a new wideband Digital Back-End (DBE) with a common block diagram, which consists basically of

1. High-speed analog-to-digital converters (A/Ds) sampling wide baseband (or higher-Nyquist-zone-filtered) analog input signals,
2. One or more stages of polyphase/FFT filter-bank, for the desired spectral resolution of output channels, and a
3. High-speed serial transceiver for selected data transport to storage and/or correlation processor.

Design of wideband DBEs is outlined, with examples of modern low-cost components: high speed A/Ds, field programmable gate arrays (FPGAs), and 0.1-10 Gb/s serial transceivers now available. For example, a dual input 512 Msample/sec DBE with 64-channel filter banks thought suitable for (e-)VLBI could be built for about $300.

1. Introduction

A paradigm shift to DBEs in radio astronomy is under way. Projects like Australia Telescope Compact Array (ATCA)[1] and Allen Telescope Array (ATA) in USA, are developing and beginning to test FPGA-based polyphase-FFT filter banks. DBEs promise greatly improved performance (aggregate bandwidth, spectral resolution, isolation, stability), essential flexibility for a wide range of experimental and operational requirements, and much lower replication, maintenance, and update costs, than traditional (now obsolescent and increasingly difficult to maintain) analog back ends. In this paper I stress feasibility of low-cost generic DBE building blocks. Study of low-cost feasibility was prompted by evident needs of both high performance and low cost in large arrays of (many thousands of) receiving elements, in particular, for LOFAR and SKA in the near and longer term respectively. This study also suggests that simple DBE building blocks should now be developed for timely, low-cost modernization of (e-)VLBI back-ends for service in the decade from 2005 to 2015. Suggested attributes of a DBE building block are:

1. **Low-cost** $500 max. (doesn't include NRE amortization)
2. **Wideband** Dual 256 MHz wide analog inputs, from 1^{st}, 2^{nd}, or 3^{rd} Nyquist zone filters, to be sampled at 512 MS/s.
3. **Digital** Polyphase-FFT filter banks (1 or 2 stages) after A/D, selection of output bands, requantization for transport, VSI-E over Ethernet formatting, etc.

[1]The influence of Dick Ferris of CSIRO ATNF on the author is gratefully acknowledged.

4. **Mini-module** 1-10 Gb/s out, "independent" parallel subsystem, 6-10 in^2, 6 W.
5. **Simple** KISS (keep it simple, stupid), or else!

To limit NRE and increase reliability it is important to minimize complexity.

For VLBI for example, I would suggest implementing only 16- or 64-channel single sideband (SSB) filter-banks for 32 16-MHz-wide or 128 4-MHz-wide outputs respectively. The former requires only half the FFT hardware resource or flow-through processing time per sample of the latter.

Also, not clearly necessary in DBE is an additional digital down converter (DDC), which is a digital quadrature mixer driven by a numerically controlled digital oscillator. The addition of a DDC could enable local Doppler compensation which may ease future distributed e-VLBI processing in PCs. If, after careful consideration, such a DDC is justified, a separate dedicated commercial DDC chip or custom FPGA version can be added.

It is important to keep DBE forward and backward compatible, as well as simple. Example 1, forward compatibility: Provide for multiple and wider IF bands and aggregate bandwidth scalability with parallel DBE mini-modules. Support wider IFs with 1^{st}, 2^{nd}, 3^{rd} Nyquist zone filters in front of parallel sampler A/Ds. Example 2, backward compatibility: Support VSI-H parallel I/O port as well as VSI-E over 1 or 10 gigabit Ethernet serial port.

2. DBE: 3 Parts, 2 Easy, 1 Hard

2.1. Part 1 (easy): Pair of Commercial-Off-The-Shelf (COTS) A/Ds

A leading candidate is MAX105, a dual 6-bit 800 MS/s-rated chip. Cost is $36.

Note, each A/D is preceded by an analog bandpass filter limiting the signal to the 1^{st}, 2^{nd}, or 3^{rd} Nyquist zone. These filters are not "formally" part of the DBE but could be physically mounted on-board. Cost is about $20 per filter in large quantities.

Table 1 lists some COTS A/Ds in order of increasing maximum sample rate along with resolution (bits/sample), cost, and power consumption parameters. MAX105 is by far the most affordable converter rated near GS/s. Its 6-bit resolution gives MAX105 an interference-to-signal ratio (ISR) of 27 dB [4], more than adequate for most radio astronomy applications, including even LOFAR in radio-quiet Western Australia. If needed, higher interference tolerance (6 dB per added effective bit of resolution), and better linearity (increase of spur free dynamic range, SFDR, from 50 to 70 dB, for example, with MAX1121) can be obtained, but at a much lower maximum sampling rate.

2.2. Part 3 (easy): Standard COTS Pluggable Transceiver, SFP or XFP

SFP (Small Form-factor Pluggable) transceivers are produced in high volume and available in many versions for:

1. Multimode fiber at 850 nm for 600 m short reach,
2. Cat5 copper for 100 m very short reach, and
3. Single-mode fiber for intermediate, long, and extended reaches from 10 to 120 km.
4. CWDM (coarse wavelength division multiplexed), for up to 16 wavelengths with 20 nm spacing from 1310 to 1610 nm have been available for 2 years.

5. DWDM (dense wavelength division multiplexed), for up to 44 wavelengths with 0.8 nm spacing, all within the C-band that can be amplified with erbium doped fiber amplifier (EDFA), have just been introduced by multiple vendors and now claim to be priced competitively with CWDM.

Plug-compatible SFP choices range from under $75 to over $750 in cost depending primarily on reach and CWDM or DWDM capability. Copper SFPs typically autonegotiate 10/100/1000 Mb/s Ethernet. Multi-rate fiber SFPs typically autotune from 0.155 to 2.7 Gb/s, OC-3 to OC-48 with forward error correction (FEC).

XFP (X=10 Gb/s small Form Pluggable, similar to SFP) transceivers are intended for 2.5 to 10.8 Gb/s operation. Non-WDM 1310 nm products for 10 and 40 km reach, costing $500 and $1500 respectively, have been introduced. Finisar demonstrated a C-band (15xx nm) DWDM XFP early in 2003. XFP is aimed at the next generation of high volume low-cost applications. The product line and its markets are expected to mature within 3 years, by which time 10 Gb/s XFP pricing should be comparable to today's 2.5 Gb/s SFP. XFP has a serial electronic interface called XFI which can be driven from a dedicated $100 Xilinx interface chip or directly from a Xilinx Virtex 2 Pro X series FPGA. This just introduced X series increases speed limit of dedicated high-speed serial ports from 3.2 to 10.8 Gb/s.

Note that candidate FPGA chips mentioned below, XC2VP20 (or VP20X), have 8 dedicated serial I/O ports which provide "glueless" physical-coding-sublayer (PCS) interfaces to SFP (or XFP) transceivers.

2.3. Part 2: FPGA(s) are Multi-Functional, NRE-Intensive, Hard Part of DBE

Replication cost of the FPGA part can be kept low enough if design adheres to KISS discipline. Adequate resources for design, technical review, detailed oversight, and rigorous testing must be provided. Proven efficient intellectual-property (ip) cores can be used where appropriate. Note, the author does not have the experience to here credibly estimate the cost of NRE including design tools and "learning curve".

2.4. Figure 1 Illustrates 3-Part and Miscellaneous DBE Cost Breakdown

Some plausible configuration options are shown. For example, 2 FPGAs could be used to support a dual 1024-point filter bank at 512 MS/s. The simplest option shown, with (a) dual A/D chip, (b) single $100 FPGA (qty. 50,000), and (c) short reach transceiver, should cost ~$250 in sufficiently high volume, and is thought to be suitable for (e-)VLBI.

3. Selection and Functions of FPGAs

3.1. Xilinx Virtex II Pro Strawman: Midsize XC2VP20-5, $100, Qty. 50,000 in 4Q04

This chip was chosen as conservative low-cost reference platform, thought to be big, versatile, and fast enough to accommodate at least the simplest envisioned combinations of primary and secondary DBE functions outlined below.

More complex DBEs with, for example, much larger, faster, or multi-stage filter banks, could be accommodated by adding one (or possibly more) identical (or at least identically packaged)

FPGAs to a mini-module PCB with layout that accepts at least 1 "extra" FPGA.

The resources of the VP20 include 20,880 logic cells, 88 dedicated 18-bit multipliers, 88 blocks of 18 Kb RAM, 8 serial "rocket I/Os", and 2 PowerPC CPUs.

3.2. Primary Function: Polyphase and FFT Filter-Banks [1,2]

A 64-point complex FFT can be computed in half real time, using a proven 64/256/1024-point Xilinx ip-core that uses 12 of 88 multipliers and one quarter of both the RAM and logic cell resources. If the chip is clocked at 128 MHz, 2 cores (<1/2 chip) could therefore keep up with complex or dual-real data sampled at 512 MS/s. A dedicated 16-point FFT would take less than half the 64-point resources.

The polyphase front-end of the filter bank – which is needed to improve adjacent output channel rejection from only 13 dB for FFT alone to > 50 dB for an appropriate effective 8-tap FIR in front of each FFT input – should not need more than 32 of the remaining 64 multipliers.

3.3. Secondary Functions

The remaining DBE functions of the FPGA are:

1. Dual 2-way demultiplexed LVDS A/D interface, input clocked at 256 MHz.
2. Selection of filter-bank output channels for transmission.
3. Requantization (compression to 1, 2, or 3 bits) of selected output channels.
4. VSI-H and VSI-E formatting of selected data for transmission.
5. Transceiver interface with or without gigE media-access-control (MAC).
6. Miscellaneous clock, time, monitor, control, and housekeeping.

Though detailed resource requirements for these functions have not yet been estimated, they should all fit, given some effort to make efficient use of remaining resources, the 2 embedded general purpose CPUs in particular.

MAC is needed if the transceiver must be able to connect directly to an Ethernet switch or router, but not if the transceiver is connected indirectly via a locally-controlled protocol-and-format-blind high-speed serial cross-point 'system' switch to an Ethernet formatting device. A simple gigE MAC ip-core uses less than 10% of a VP20.

4. Bottom Line

A Digital Back-End (DBE) building block (mini-module) can now be designed to:

- Cost about $300 for VLBI, about $500 for LOFAR
- Convert two 256-MHz- wide baseband (or higher Nyquist zone) inputs to 32 16-MHz-wide or 128 4-MHz-wide output channels for VLBI (but LOFAR needs '2^{nd} stage' filter-bank)
- Select and format arbitrary subsets of these channels for transmission using VSI-E over Ethernet serial protocol or VSI-H parallel intermediate interface.
- Be an independent parallel subsystem, managed through its serial receiver via either an Ethernet or "system" switch as described above.

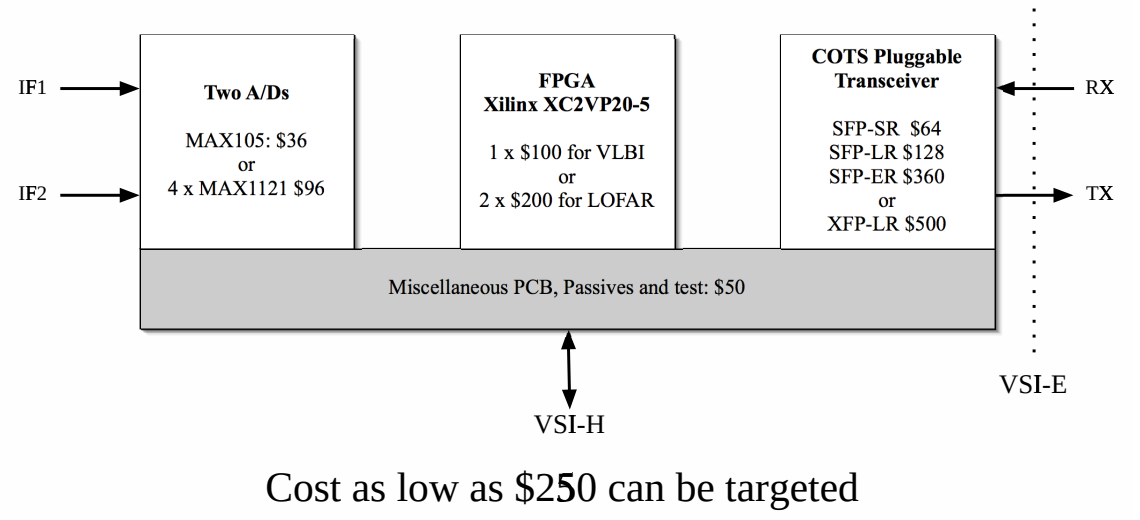

Figure 1. DBE Mini-module

Table 1. COTS A/Ds

Description	Gsamples/ second	bits/ sample	$	Watts
AD9430	0.21	12	108	1.2
MAX1124	0.25	10	50	0.5
MAX1121	**0.25**	**8**	**24**	**0.4**
$\frac{1}{2}$MAX105[3]	**0.8**	**6**	**18**	**1.3**
MAX104	1.0	8	400	5.2
MAX108	1.5	8	600	5.2

References

[1] Ferris, R., High Speed Samplers and Digital Filters, June 2003 presentation.

[2] Crochiere, R. E., Rabiner, L. R., Multi-rate Digital Signal Processing, Prentice Hall 1983.

[3] Hinteregger, H. F., Summary of Initial Tests of MAX105, Haystack LOFAR Memo #16, 2 February 2004.

[4] Hinteregger, H. F., Speed, Resolution and Linearity of A/Ds for LOFAR, Haystack LOFAR Memo #15, 2 February 2004.