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DBBC – A Flexible Platform for VLBI Data Processing

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Abstract

The development of the first version of DBBC is complete and an extended testing phase is planned for 2006. The instrument is a flexible tool that realizes a complete analog VLBI pre-recording terminal in digital technology, with the additional capacity to process data in a different fashion for multiple narrow or fewer very wide band channels without changing any hardware part. We show a description of this instrument, report on the performance with the present implementation, and point out the potentiality for a different implementation using the same hardware. Moreover a description of the second version is given with some details on new hardware parts for additional functionalities, such as RFI mitigation, and AD sampling at the receiver site.

1. Introduction and General Description

The main idea behind the 'DBBC' project is to replace the existing VLBI terminal with a complete and compact system to be used with any VSI compliant recorder or data transport. Moreover the cost has to be limited by making use of commercially available components.

Hardware programmability is a fundamental feature in order to optimize the architecture for a particular, requested functionality the instrument, because different performance involves a different number of gates necessary to perform the required functionality. Under these assumptions, maximum input and output data rates are the limitation and they have to be set so that they satisfy the present and possible future requirements.

The new development needs to be fully compatible with the existing terminals and correlators in order to minimize the efforts to introduce them at the stations and to eliminate any modification at the correlator side, still maintaining the possibility to upgrade to a new class of correlators. The possible upgrades have to be mostly software in order to avoid modifying any hardware part, to save cost and to simplify the operations, so that programmable hardware is the main component. However, a hardware upgrade will still be possible, because a standard in the connection of the different elements is defined.

The entire project is based on a flexible architecture, composed of one or more FPGA boards as computation elements, placed in a mixed cascading/parallel structure, so as to guarantee a parallel usage of data input and a shared parallel output data flow.

In a DBBC a single system unit is composed of four RF/IF Input in the ranges 0.01-512 MHz, 512-1024 MHz, 1024-1536 MHz, 1536-2048 MHz, and 2048-2100 MHz with each of them feeding a 1.074 GHz clock sampler. Then four polarizations or bands are available for a single group of output channels. A group of 64 channels is able to handle a shared combination of channels coming from the four bands, supporting two VSI output connectors as output.

Multiple architecture can be used to take advantage of adopting fully re-configurable FPGA Core Modules, where one of such modules is an autonomous board populated with an appropriate number of gates, fed by any of the four IFs, and sharing the output data bus. Narrow or wide bandwidth channels per module can be assigned, maintaining the maximum number of gates provided by the Core Module. Modular realization for a stack processing is provided, which implies the use of one or more Core Modules for achieving a higher number of gates and then more processing capability. The input bus is cascaded, with very low skew, between modules.

An analog monitor, produced by DA conversion, has been added for testing purposes, in order to be able to evaluate with a common spectrum analyzer the contents of the different channels and their performance. This has been proved particularly useful in order to adopt standard equipment normally in use at a radio-telescope. Field System support is required to configure the different modules and allow standard settings, while still getting total power measurements of the converted channel. A limited effort should be assured on the FS side to include the support for the DBBC due to the implicit FS-like structure of the commands the DBBC is able to recognize.

Different configurations can be supported to obtain similar, but not identical, functionalities, such as SSB down converter, wide band parallel FIR, and poly-phase FIR/FFT, to mention a few. The possibility to independently tune different channels, and to have them filtered at different bandwidth, though an obvious feature in the analog implementation, is not so obvious a solution for the digital implementation, as different solutions could appear to be more appropriate. For this reason the project allows implementation of different architectures and the ability to change them at convenience.

A Core Module can handle a maximum input bandwidth of more than 34 Gbit/s, and a maximum output bandwidth of 8.192 Gbit/s. Two high rate buses are present, named HSI and HSO, respectively, with the addition of a further Control/Configuration/Monitor bus, named CCM.

2. System Components

In Figure 1 the DBBC is shown, while a schematic view of the instrument is visible in Figure 2. Signals coming from the receivers trough the Conditioning Module are kept at the proper level before the sampling process.

The ADBoard (Figure 3) performs the analog-to-digital conversion at a rate of 2^{30} Hz. Four of these units are able to feed four IFs with 8-bit representation in the processing units, the Core Module boards (Figure 4). The maximum number of such FPGA boards is 16 in a stack configuration. The FiLa (First/Last) board (figure 5) opens and closes the chain. This board is indeed used in the initial and final part of the stack to perform more functions: 2 VSI interfaces, DA monitor, Timing synchronization and Clock Synthesizer, Communication, JTAG channel.

The FPGAs Core Configuration represent the firmware to perform the desired functionality, such as the SSB base band conversion. Different architectures can be used because of the full programmability of the module.

The Power Distributor board generates the supply voltages for each board of the chain. The software, able to manage the entire functionality of the DBBC, is run on a compact PC board with the help of two PCI commercial interfaces. System Management Software is Field System oriented, so that standard commands to set and use the instrument are Field System-like, requiring a minimum effort to integrate the DBBC into that environment.

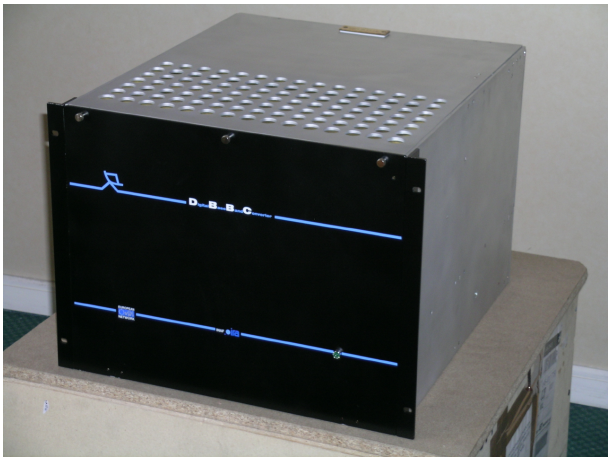

Figure 1. DBBC Back-end System.

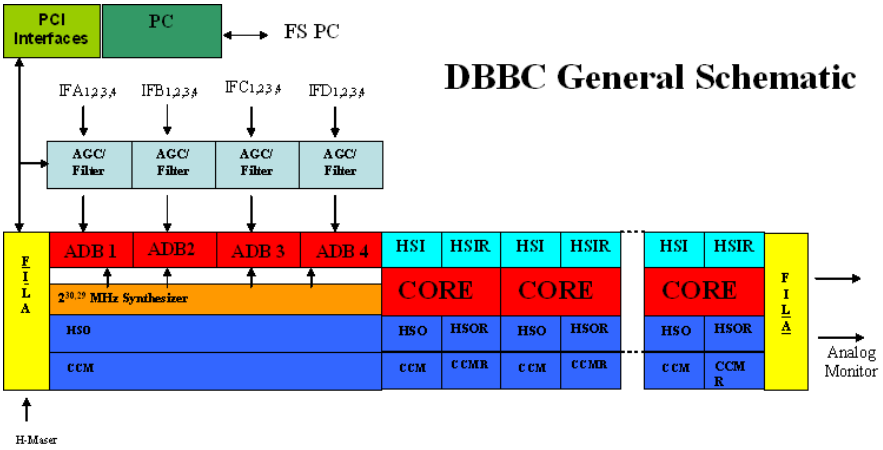

Figure 2. DBBC schematic functional representation.

3. Configuration

Different architectures can be used in the Core Modules, having different performance and behaviors. One possible configuration is the DDC digital down converter in the sense of the classical implementation. In such a solution a direct SSB conversion is typically performed between a high data rate sampled IF band and a lower data rate base band. One or two channels are generated for each converter, as in the analog implementation. Important differences, greatly improving the performance are present: the local oscillator is a Numerically Controlled Oscillator (NCO), the mixer is complex as Look Up Table multiplier, the low-pass band filters are Finite Impulse Response (FIR). Decimation circuitry is adopted because of the high ratio between IF and output data rate and is performed with multirate/multistage FIR. Digital Total Power (DTP) measurement at base band level is adopted; Rescaling/Gain Control (RGC) is adopted for dynamic range control and final data representation. The tuning step is 1 Hz, giving the possibility to finely tune the receiver

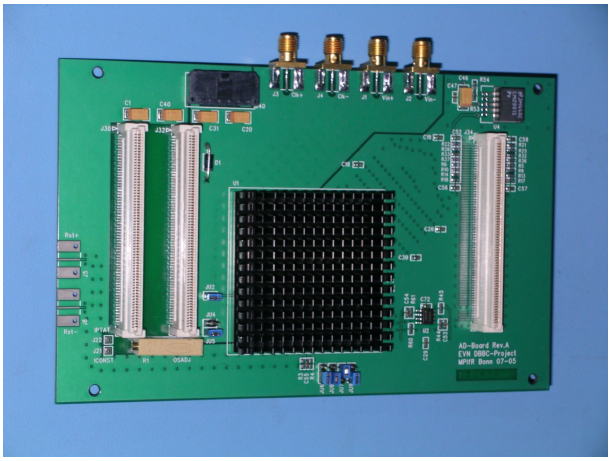

Figure 3. ADBoard - Sampler board 8-bit at 2^{30} Hz clock frequency.

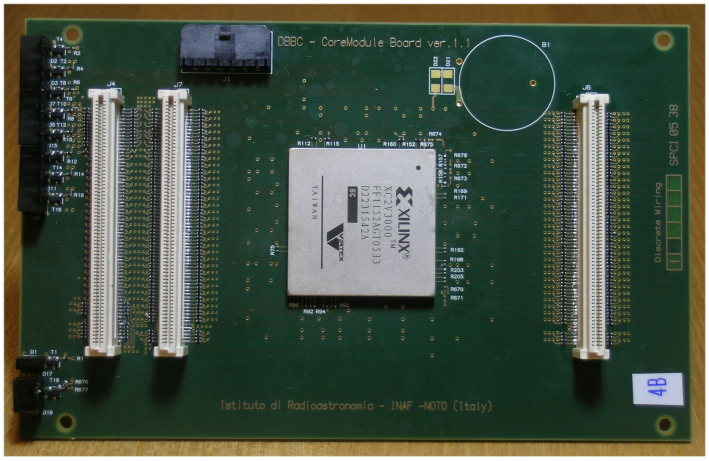

Figure 4. Core Module Board is the processing element, with three high data rate I/O bus.

for spectroscopy or any other precise frequency settings. Narrow bandwidth typically adopted is defined for this project in the range: 16, 8, 4, 2, 1, 0.5, 0.25 MHz. Output data rate is 32 or 64 MHz at present in order to be able and fit with the standard, now adopted VSI-H data rate. A 128 MHz clock rate is the maximum supported.

4. Upgrade

Testing with real observations started with mDBBC (IRA-SHAO agreement): fringes have been detected on both analog-digital and digital-digital baselines. First analog-digital fringes have been detected on the Seshan-Urumuqi baseline on Nov 23, 2004, while first digital fringes were detected on the Noto-Seshan baseline on Feb 2, 2005.

2006 will be dedicated to an observation–optimization process. Moreover, an update program for improving performance is under way. It includes FPGA Virtex4 device testing for double

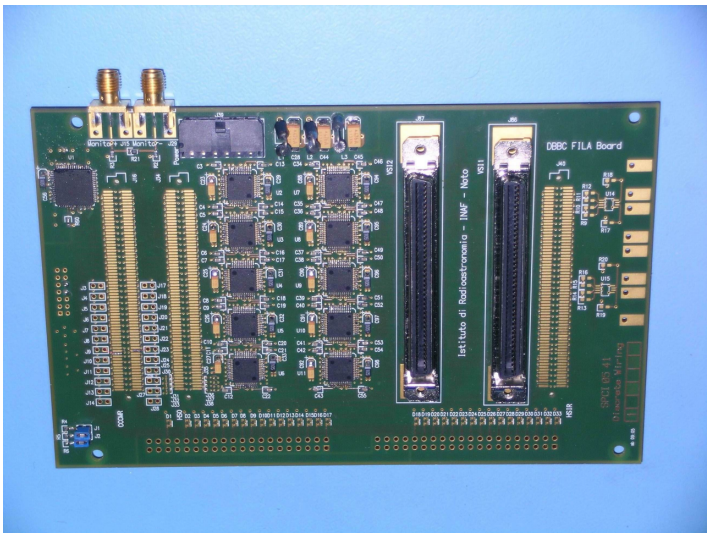

Figure 5. FiLa Board - Support two VSI interfaces, DA converter, PC communication, JTAG programming.

processing clock and price reduction; Faster AD sampler for increasing the input bandwidth; AD sampler placed inside the receiver and sampled data sent through an optical fiber; RFI Mitigation Board; and the first Core Module (same hardware) acts as RFI processor in transferring the pure sampled data with proper configuration.

5. Conclusions

The DBBC system is a highly flexible instrument because it is able to produce independent tunable channels for full compatibility with the existing acquisition system and correlators. One Core Module board replaces a BBC module. Combination of up to 4/16 IFs in a single module is possible. The DBBC system is also able to handle an equi-spaced multichannel configuration for producing contiguous non-tunable channels. A Core Module board is able to produce multiple channels. More solutions are possible within the same system using software selection. A minimal architecture is composed of 1 ADBoard, 1 Core Module (multichannel configuration, or any other), 1 FiLa board (VSI interface, DA converter, etc). A maximal architecture in one system is composed of 4 Conditioning Modules, 1 FiLa board, 4 ADBoards, 16 CoreModules, 1 FiLa board, PC and PCI interfaces. Such wide range of hardware and software conditions allow one to assemble a low cost system with the needed performance.

References

[1] G. Tuccari, Development of a Digital Base Band Converter (DBBC): Basic Elements and Preliminary Results In: New Technologies in VLBI, Astronomical Society of the Pacific Conference Series, Vol. 306, p.177-192, 2004.