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FPGA Implementation in DBBC

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Abstract

As one of the main equipments for VLBI stations, the VLBI data acquisition rack takes on the tasks of frequency selection, data collection, data encoding, data recording and etc. As the main part of this equipment, Analog Base-band Converter (Analog BBC) has very complex analog circuits which is obsolete and very expensive. This paper mainly describes the use of digital integrated circuits (FPGAs: Field Programmable Gate Array circuits) to realize the corresponding algorithm called Digital Base-band Converter (DBBC) to take the place of the analog BBC. A simplified version of the DBBC named miniDBBC and achieved in a collaboration between China and Italy, produced some experimental results in real VLBI observations.

1. Introduction

The speed of circuits and resource capacity in Field Programmable Gate Array circuits (FPGAs) has had a rapid development in recent years. In DBBC, we also take advantage of FPGAs to realize our algorithm and make it a very flexible platform for VLBI data processing. At present, the type of FPGA we use in digital BBC is XC3000 which is the product of Virtex-II series of Xilinx company and the speed grade is 6. Later we will upgrade to Virtex-4 series, the newest product for Xilinx. There are two kinds of possible configurations considered in FPGAs. One is called the digital down converter, the other is equally spaced multi-channel configuration. With the first configuration, we could fulfill all the functions of the existing analog BBC. In the paper, the digital BBC is analyzed first in the overall architecture and then in detail (sections 2 and 4). The experimental results are presented in section 3.

2. Algorithm of Digital Down Converter Configuration in FPGA

The BBC is required to band selection in wide band signal and suppress the undesired sideband to generate single sideband signal. The digital down converter configuration is shown in Figure 1. The analog signal is digitized by an A/D sampler and then input to FPGAs. Figure 1 shows a channel of DBBC to implement in FPGA. Prior to digital filtering, the digital signal is down-converted by multiplying it with the Direct Digital Frequency Synthesizer (DDS). Here the DDS is used to generate the local oscillation signal. The transformation generates two signals in quadrature. The I and Q signals are filtered separately, differentially phase-delayed by 90 degrees by means of a Hilbert filter, and then combined together. Finally the combined signal is passed through the digital shape filter determining the band-pass shape. Several channels can be in existence in one device at the same time depending on how much resource in FPGA. These channels can work independently.

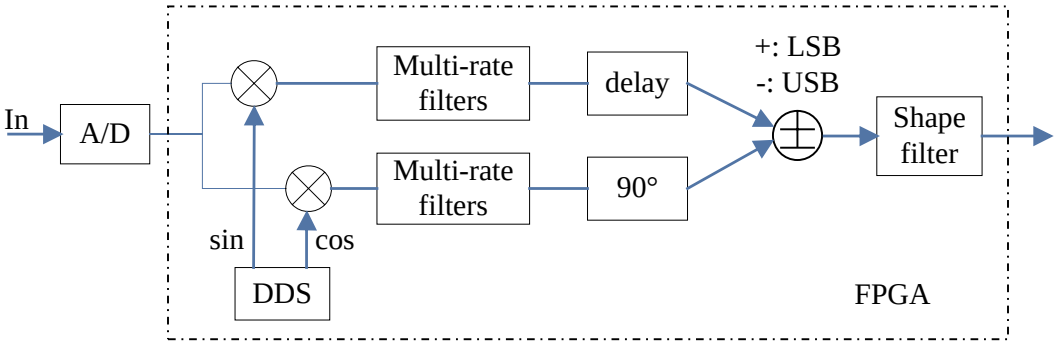

Figure 1: the digital down converter configuration

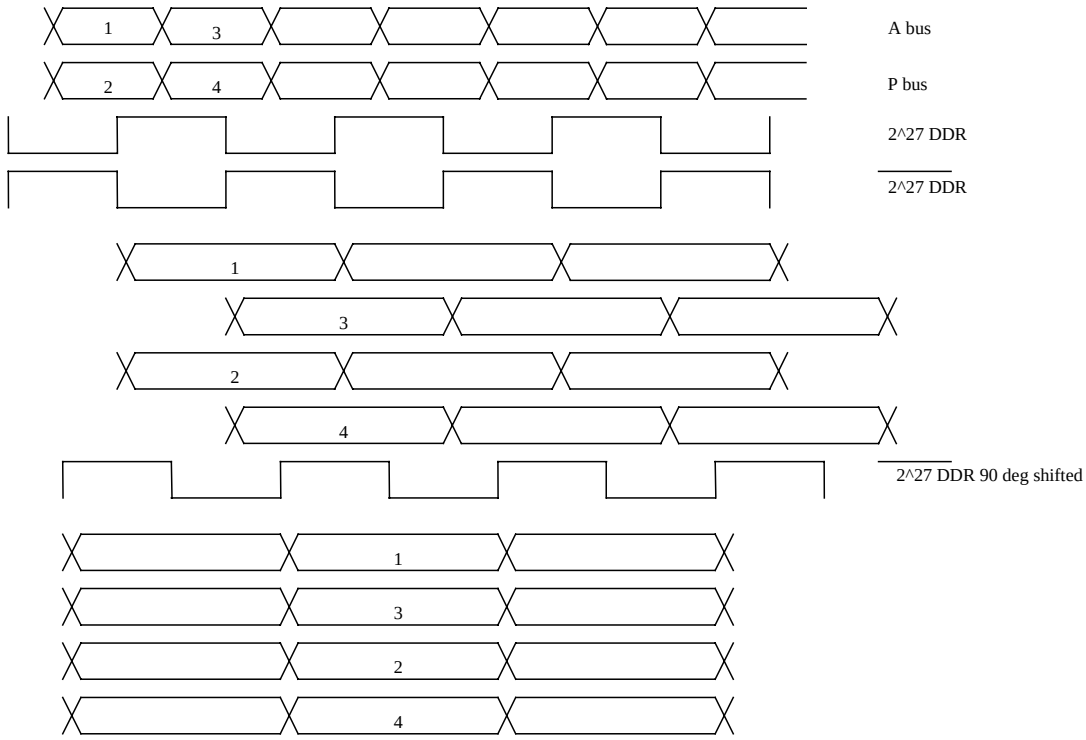

Figure 2: DDR mode and processing with 4-bus parallel in FPGA

At present, the speed of input/output port in FPGA could reach very high while in the double data rate (DDR) mode, the performance of high-speed data transfer will be double. In FPGA the input signals are serial-to-parallel immediately, and then they are processed at relative low speed to ensure the circuits' reliability. In Figure 2, 2-bus data (time division) from A/D sampler are clocked by rising and falling edges—producing 4-bus data in parallel while adopting a clock with 90-degree shift. With the multi-bus data in FPGA, the digital filters and down-converter also

need to be implemented in parallel. A poly-phase filter is adopted to realize digital filtering while parallel DDS with different initial phase are used. The algorithm of parallel DDS implementation is as follows.

$$F_{cir} = \frac{f_{out} \cdot 2^{B_{\theta(n)}}}{f_{clk}} mod(2^{B_{\theta(n)}}) \tag{1}$$

$$\Delta\phi = 2\pi f_{out} \cdot \frac{1}{f_s} = \frac{2\pi}{M}\frac{f_{out}}{f_{clk}} \tag{2}$$

Where F_{cir} : Phase increment

$\Delta\phi$: Initial phase difference between two branches

f_{clk} : Clock frequency in FPGA

f_{out} : Digital local oscillator frequency needed to generate

$B_{\theta(n)}$: Bit-width in phase accumulator

f_s : Sampling frequency

M : Number of the parallel branches

3. Experimental Results of MiniDBBC

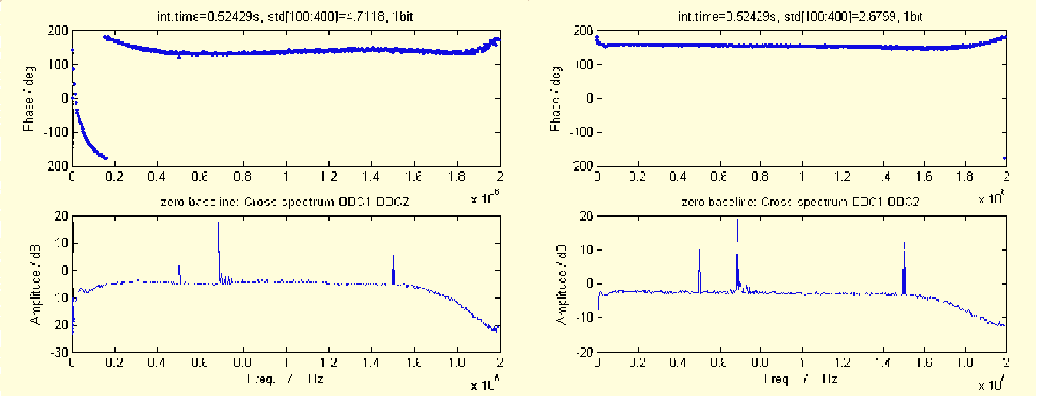

Figure 3: The zero baseline fringe

The DBBC has the simplified version, called miniDBBC and being the result of a collaboration between China and Italy which produced some experimental results in real VLBI observations (Fig 3, Fig 4). Figure 3 shows the fringes of the zero baseline observed in Sheshan. The left picture is the fringe correlated with miniDBBC and analog BBC. The right one is produced by correlation with two analog BBC. From the left picture, we can see an obvious nonlinearity in phase near the area of zero frequency (the big jump is a 360 degree wrap). To determine the reason, we measured the analog BBC and miniDBBC's phase characteristic using PCAL method. We found that the miniDBBC's phase is linear, but that there is a nonlinearity in the analog BBC's phase whose shape is similar to the left drawing. The different channels' performances of analog BBCs are almost identical, so the fringe of two analog BBCs is almost flat. Figure 4 is the fringe of 3C454 radio source correlated with data by Sheshan using miniDBBC and Urumqi using analog BBC.

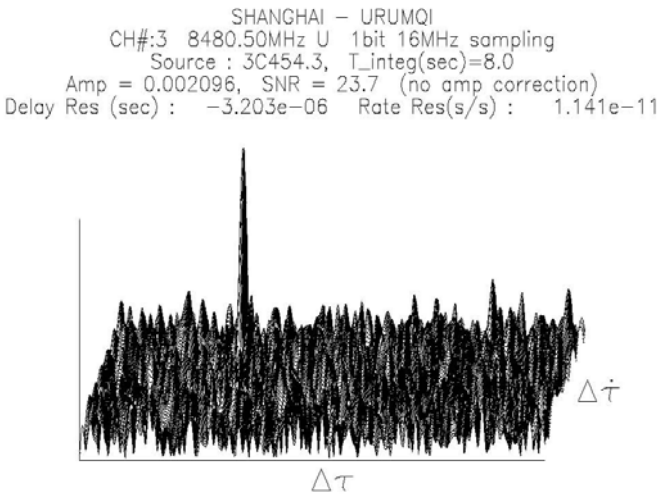

Figure 4: The fringe of radio source 3C454.3

4. Other Possible Configuration Algorithm

Using FPGA makes DBBC hardware become a highly flexible platform. We can download different configurations to implement different functions or upgrade. There are other configurations for DBBC, such as poly-phase filter + FFT (Fig 5). The advantage of this configuration is that many channels could be realized at the same time and saving the resources in FPGA. The disadvantage is that these channels are not independent; the band space between two neighboring channels is equal and cannot be tuned separately.

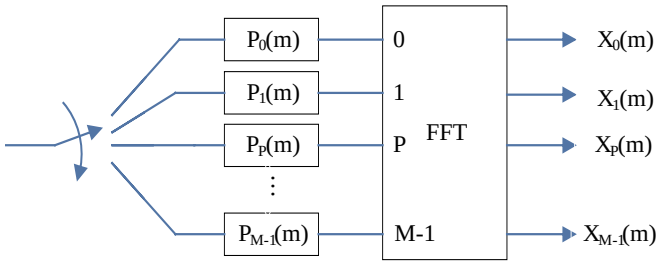

Figure 5: The poly-phase filter + FFT configuration

Acknowledgements

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