Zhijun Xu et al.: Real Time Correlator in FPGA, IVS 2006 General Meeting Proceedings, p.89–92
http://ivscc.gsfc.nasa.gov/publications/gm2006/zhijun

Real Time Correlator in FPGA

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Abstract

Real time correlator is very important for the Chinese e-VLBI development and the China Luna project. Taking advantage of the Field Programmable Gate Array (FPGA) technique, we developed a three stations real time hardware correlator at Shanghai Astronomical Observatory (SHAO). This paper briefly describes the architecture of the real time correlator and presents some results from real observation data.

1. Introduction

The Field Programmable Gate Array (FPGA) technique developed very fast in recent years. It can realize very complex algorithms and control logic now. The real time hardware correlator developed at Shanghai Astronomical Observatory also takes advantage of the FPGA technique. At present, the FPGA chip used is an XC4VSX35 which is Virtex-4 SX Platform FPGA series chip produced by Xilinx Company. Later we will upgrade the correlator to five stations using the same chip or the higher version XC4VSX55. In this paper, the main characteristics and the details of the overall architecture are described. Then the correlator results are presented.

2. Real Time Correlator

2.1. Characteristics

The correlator we developed is a three stations FX correlator with one IF, which will later be upgraded to 5 stations with eight IFs. The data rate is up to 32 mega samples per second with 1 or 2 bits per sample. The integration time can be 32.768 milliseconds to 1 hour, typically it is 5 seconds. The input data format can be Mark IV or Mark 5, the VSI interface is also under development. The data sources are from disk array or via network. Outputs of the correlator are via net or saving to disk files. The fringe searcher and Phase Cal are still software version and later will also be implemented in hardware.

2.2. System Architecture

As shown in Figure 1, each station (in three cities, Shanghai, Urumchi and Kunming) has a Mark 5 recorder. During observation, the data from Mark 5 recorder are transfered via network to the Play Back Device (PBD) computer. Each PBD has 1G DDR RAM as FIFO, the data stored in the RAM is sent to each Play Back Interface (PBI) via a 7300A high speed digital I/O card. The PBI decodes Mark IV or Mark 5 data and sends outputs to the FFT&MAC board. One FFT&MAC board can process one IF data; 8 IFs shall have 8 boards. The FFT&MAC

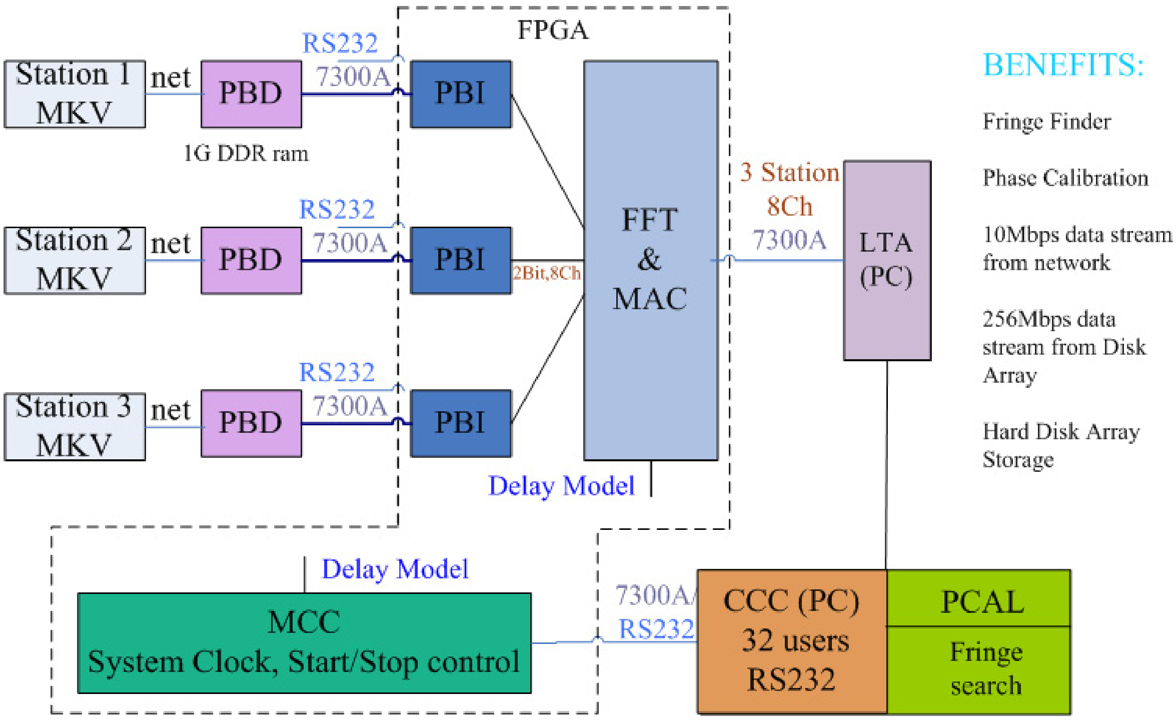

Figure 1. Architecture of the Correlator.

board has integer bit delay, fringe stopping, Fast Fourier Transform (FFT), Fractional Sample Time Correction (FSTC), multiple and accumulate (MAC) functions. The delay models needed for integer bit delay, fringe stopping and FSTC process on the FFT&MAC board are sent from the Master Control Card (MCC). Also, the MCC sends the system clock, start/reset control signal to the each PBI and FFT&MAC board. The output data from the FFT&MAC board are sent to the Long Term Accumulator (LTA) computer via 7300A high speed digital I/O card. The final results are displayed in real time on the monitor. The result data are saved in FITS format or sent to the Control Card Computer (CCC). The CCC will process fringe searcher and Phase Cal. Also, it generates the delay models and control commands to the MCC controlling the overall correlator.

The entire three stations correlator system consists of five computers and five FPGA boards. The five computers are three for Play Back Device (PBD), one for Long Term Accumulator (LTA) and one for Control Card Computer (CCC). The five FPGA boards are three for Play Back Interface (PBI), one for FFT&MAC board and one for Master Control Card (MCC). Both PBI and MCC boards are using FPGA chip XC3000 which belongs to the Virtex-II product series of Xilinx Company. The FFT&MAC board is using the XC4VSX35 chip and the speed grade is 10.

3. Results

Figure 2 and Figure 3 are the results from real observation data. Figure 2 shows the fringe result of the Shanghai—Urumchi baseline of TC-1 satellite observations with integration time of

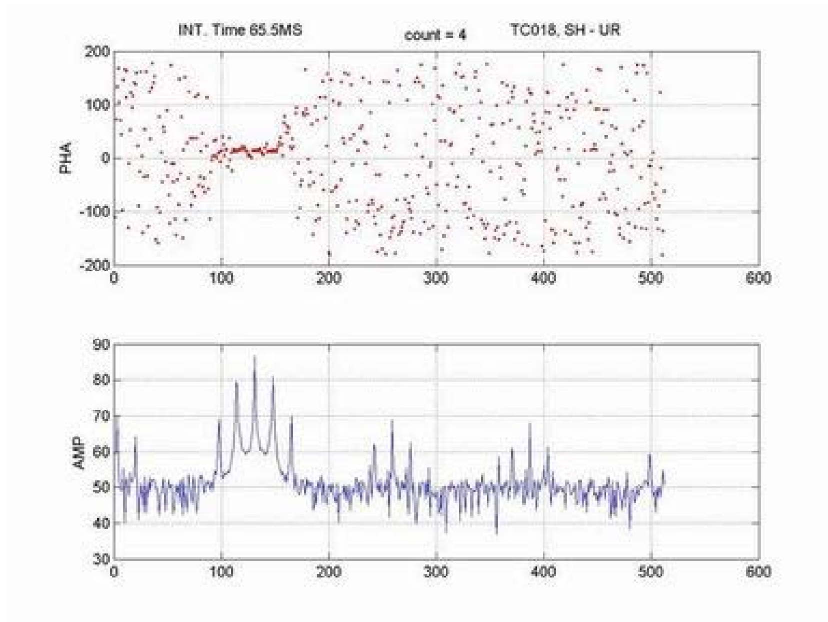

Figure 2. TC-1 results with integration time of 62.5 ms.

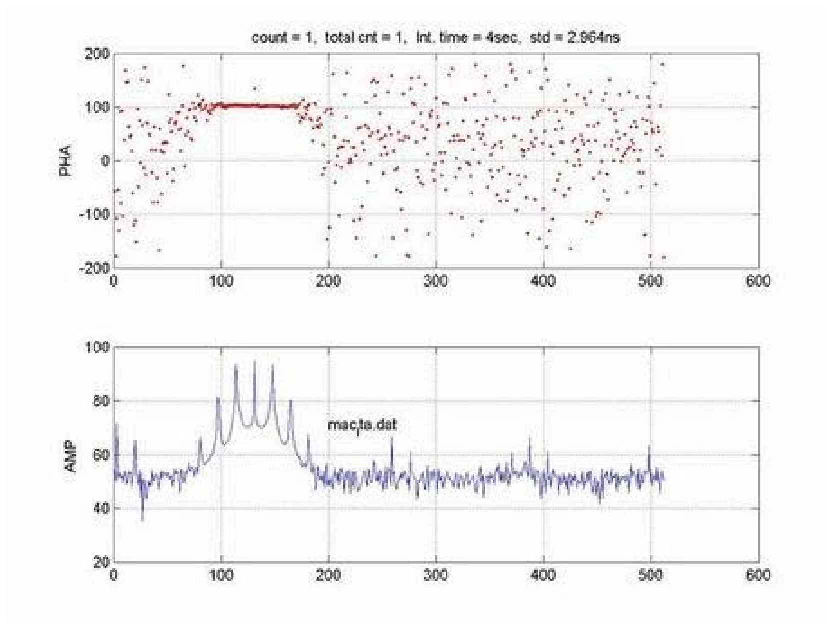

Figure 3. TC-1 results with integration time of 4 second.

62.5 ms, Figure 3 is the result of the same observation with integration time of 4 second.

References

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