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The IAA RAS 6-station VLBI Correlator

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Abstract. The development of the 6-station hardware XF correlator at the IAA RAS has almost been completed. The correlator will be used for processing national geodetic VLBI observations. The correlator simultaneously processes VLBI signals from 6 stations (15 baselines) with 16 frequency channels per baseline. The correlator input signals are two-bit VLBI VSI-H signals with 32 MHz maximum clock frequency and maximum data rate of 1 Gbps. The correlator is going to be equipped with Mark 5B playback terminals. We plan to complete and test the correlator in 2009.

1. Introduction

At present the development of the new 6-station Astrometric Radiointerferometric Correlator (ARC) has finished and the production was started. The main goal of ARC is the processing of the national geodetic VLBI sessions. The ARC features are:

- simultaneous processing of VLBI signals from 6 stations (15 baselines);
- 16 frequency channels per each baseline;
- total processing 240 frequency channels;
- two-bit VLBI signals processing;
- 32 MHz maximum clock frequency;
- maximum data rate from each station — 1 Gbps;
- VSI-H input signals;
- Mark 5B playback terminals.

2. Basic Module of Correlator

The main part of ARC is called Basic Module of Correlator (BMC). This device carries out all the hardware data processing. BMC enables processing of

16 single-baseline frequency channels of a typical geodetic VLBI observation. BMC includes 16 correlation units which are a single-baseline single-channel XF correlators for calculating 64 complex delays and picking up phase-cal tones.

BMC is based on FPGA technology. Its schematic is shown in Fig. 1.

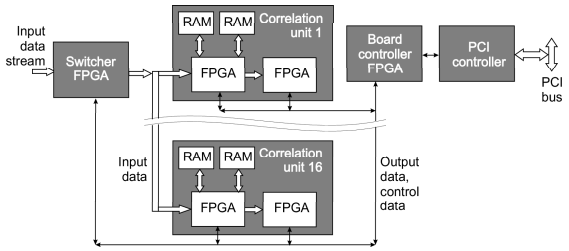

Figure 1. BMC schematic

BMC consists of correlation units, Switcher, BMC controller, and PCI controller. BMC's input data stream is separated and distributed to correlation units with the Switcher, which performs multiplexing of 64 input data bits and 2 valid bits to 16 correlation units. Each unit receives 6 bits – Sign, Mantissa and Valid for each station.

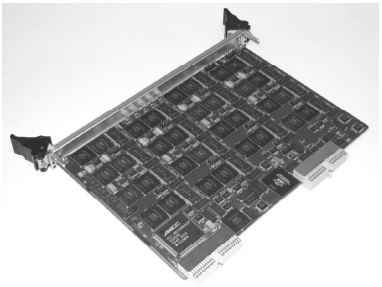

Figure 2. Single BMC board

Figure 3. 4 BMC boards in Compact PCI crate

BMC is a PCI board and controlled through PCI bus. Control commands and model parameters passes to correlation units and Switcher through PCI controller chip and BMC controller. Measured correlation data passes to the control computer through BMC controller, PCI controller and PCI bus. Each correlation unit consists of two FPGA chips and two RAM chips. The data processing algorithms are implemented as FPGA programs. BMC is a Compact PCI 6U front plug-in board. In Fig. 2 and 3 the BMC and 4 BMCs mounted in Compact PCI 6U crate are shown.

3. ARC Hardware Structure

The 6-station ARC includes 6 Mark 5B terminals and 15 BMC. BMCs are installed in four Compact PCI 6U crates. The Signal Distribution and Synchronization System (SDSS) distributes signals from Mark 5B to BMC, so as each BMC receives signals from two Mark 5B. Besides, the SDSS generates and sends synchronisation signals DPSCLOCK and DPS1PPS to Mark 5B terminals.

ARC contains one personal computer with the user interface. Crates with BMCs, Mark 5B terminals and a personal computer are joined into the local correlator network. ARC hardware block diagram is shown in Fig. 4.

SDSS has several types of Compact PCI boards in its constructions. SDSS block diagram is shown in Fig. 5.

The Generator of Synchronization Signals (GSS) produces DPSCLOCK and DPS1PPS signals.

The main part of data stream distribution was performed by Signal Distribution Modules (SDM). Boards receive synchronization signals from the GSS and passes to the Mark 5B terminals. The SDM produces five copies of Mark 5B output data stream from each one of the Mark 5B terminals and then distributes these streams to the BMCs. Each one of the 32-bit (and service bits) parallel LVDS-standard Mark 5B data streams is converted into 4-bit serial LVDS data stream enhancing data transfer characteristic.

The Interface Module of Correlator (IMC) receives 2 serial data streams coming from 2 SDMs, converts data streams into 2 parallel 32-bit TTL data streams and transfers them to the BMC.

SDM and GSS are Compact PCI 6U front plug-in boards. IMC is the Compact PCI 6U rear panel I/O board.

4. ARC Software

ARC software is a distributed system with parts in personal computer and in the four Compact PCI 6U crates. Crate coordination, Mark 5B control and data transfer are made via the local correlator network. The software includes a task-making program, ephemeris program, hardware control program and postprocessing program. At present the correlator results are available as NGS card files.

5. BMC Prototype

The prototype of BMC was developed at IAA RAS in 2004. This small device, named MicroParsec, is able to process two frequency channels simultaneously. It is connected to the S2-PT terminal working in VSI-H mode.

From 2004 to 2006 the 3-station correlator based on these devices has been developed. Now it is used for processing national VLBI experiments carried out with stations Badary, Svetloe and Zelenchykskaya and recorded with the

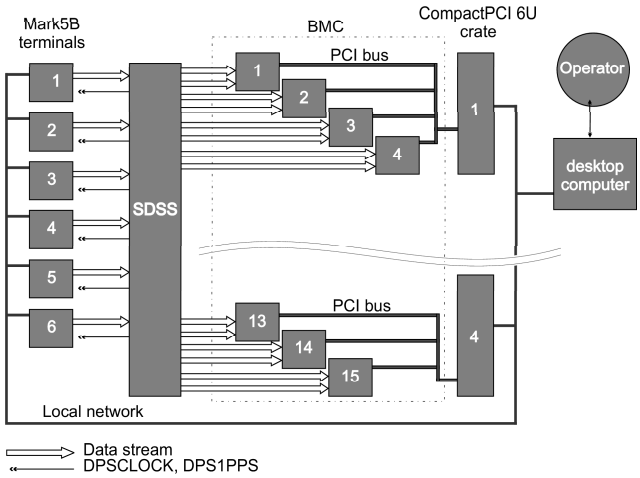

Figure 4. The ARC hardware block diagram

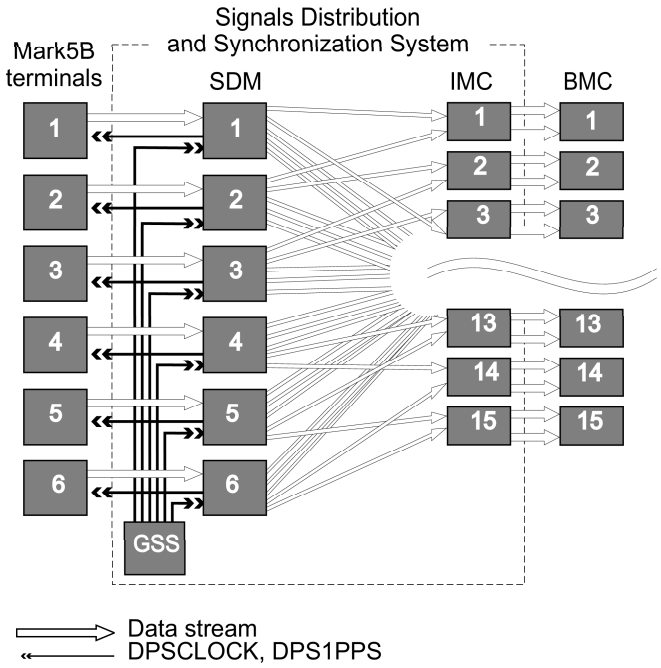

Figure 5. SDSS block diagram

S2-terminals. MicroParsec device and correlator are shown in Fig. 6, 7.

Figure 6. 24-channel correlator based on MicroParsec devices

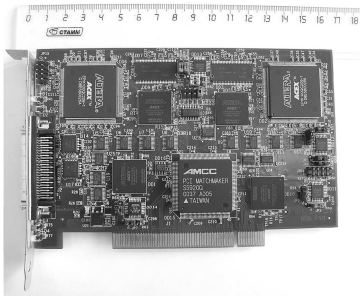

Figure 7. Single MicroParsec device

6. Conclusion

BMC development was started in 2004. To date number of experimental BMC devices have been produced. The production of the correlator prototype has been started. We plan to have a single-baseline ARC prototype in 2008. We plan to complete and to test the complete correlator in 2009.

References

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