### Progress in Technology Development and the Next Generation VLBI System

# Progress of Wideband VLBI Digital System Development at SHAO

Xiuzhong Zhang <sup>1</sup>, Wenren Wei <sup>1</sup>, Ying Xiang <sup>1</sup>, Bin Li <sup>1</sup>, Fengchun Shu <sup>1</sup>, Renjie Zhu <sup>1</sup>, Zhijun Xu <sup>1</sup>, Zhong Chen <sup>1</sup>, Weihua Wang <sup>1</sup>, Weimin Zheng <sup>1</sup>, Zhuhe Xue <sup>1</sup>, Q. Ling <sup>1</sup>, R. Zhao <sup>1</sup>, Jingling Wang <sup>1</sup>, Qingyuan Fan <sup>1</sup>, Yusufu Aili <sup>3</sup>, Huihua Li <sup>1</sup>, Y. Wu <sup>2</sup>, L. Chen <sup>2</sup>, J. Luo <sup>2</sup>

- 1) Shanghai astronomical Observatory, Chinese Academy of Sciences, China
- <sup>2)</sup> Graduate University of the Chinese Academy of Sciences, China
- <sup>3)</sup> Urumqi Station, National Astronomical Observatory, Chinese Academy of Sciences, China

**Abstract.** Several wideband VLBI devices, such as wideband DBBC, and a 5-station correlator have been developed at Shanghai Astronomical Observatory. The design concept and the applications of these devices are reported in this paper.

# 1. Project Overview

In support of the Chinese Lunar Project, in the past two years two new VLBI stations were built in China. One of them is a 50 m telescope, which is located in Mijun near Beijing. The other is a 40 m telescope, which is located in Kunming in southern China. As VLBI station, the VLBI equipment such as the data acquisition system, are needed for these two VLBI stations. Also the correlator is required for data reduction. As a project requirement, we started to develop a 5-station correlator and a data acquisition system in the past several years. The 5-station correlator was completed in 2006. The Data Acquisition System (DAS) with digital base band converter is under development now.

#### 2. The Data Acquisition System

The DAS is the key equipment at a VLBI station. The traditional DAS with analog Base Band Converter (BBC) are used in most VLBI stations in the world now. Unfortunately, this type of DAS is not manufactured anymore. The new type DAS with digital BBC comes slowly onto the market. After long time discussion, the SHAO started the development of a DAS with digital BBC in the beginning of 2007. The system will be operated at 4 Chinese VLBI stations by the end of 2008. The new type DAS is called NDAQ. It is fully compatible with the traditional DAS, which currently runs at the VLBI stations. But the total bandwidth of NDAQ is 4GHz. NDAQ has two data output interfaces. One is Mark IV interface and the other is VSI interface. With different IP core, the NDAQ could be compatible with DBBC and DBE, which are being developed by EVN and Haystack Observatory, respectively. NDAQ has the following characteristics:

- use 5 MHz as standard frequency signal input,
- use 1 pps as a time signal input,
- 4 IFs, the bandwidth of each IF may be 512 MHz or 1024 MHz selectable,
- two MK4 interfaces to MK4 Formatters or two VSI to MK5B/C Disk Arrays,
- fully compatible FS interface of traditional DAS (hardware and software),
- PCAL and auto-spectrum output,
- two channel DAC for channel output signal monitor,
- PCI interface for control.

Fig. 1 shows the diagram of NDAQ. There are three parts in NDAQ. They are RF AGC, Digital Part, and Output Module.

#### 2.1. RF AGC

The Automatic Gain Controller (AGC) amplifies the IF signals from the standard astronomical receiver to the optimum power level for the subsequent high-speed digital A/D converter. One AGC unit contains four separate channels which share one digital interface board and could be synchronously processed. Each channel can accept either lower IF (DC 512 MHz) input or higher IF (512 MHz, 1024 MHz) input by setting the internal switches. Each channel has maximal 50 dB gain and above 60 dB dynamic range. The 0.25 dB finest attenuation step and less than 50 ms close-circle adjusting time allow the AGC unit to provide stable output signals. The AGC unit and the 1024 MHz synthesizer are integrated in a 3U EMC shielding metal box. The AGC unit can be remote monitored and controlled through a simple RS-232 interface.

# 2.2. Digital Module

The main part of the digital module's hardware consists of four FPGA-based processing boards, each one containing one Atmel AT84AD001B Analog-

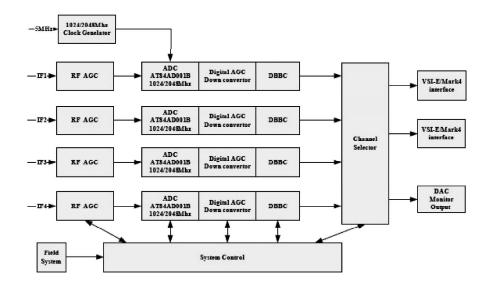


Figure 1. Diagram of NDAQ

to-Digital Converter (ADC), four Xilinx XC4VLX160 Virtex-4 FPGAs with 152k configurable logic cells, and one Xilinx XC4VFX60 integrated with two PowerPC CPU cores. The board's size is 6U that could be installed in the corresponding commercial chassis with cPCI interface backplane. The Atmel ADC on the board could work on 1024 Msamples/sec or 2048 Msamples/sec (interleave mode). With the different firmware in the four XC4VLX160, the NDAQ could implement different functions. The Xilinx PCI IP core (OPB-PCI) and communication program are in the XC4VFX60 that could configure the 4 XC4VLX160 and monitor the board state.

#### 2.3. Output Module

The output module selects a usable data channel to the output interface. The PCAL fetch function and two DAC channels in the output module. After zero baseline tests at Seshan station, two NDAQ test models were integrated at the Seshan and Nanshan stations to start with regular test observations followed by VLBI observations of CE-1. Some results are shown in Fig. 2 and Fig. 3.

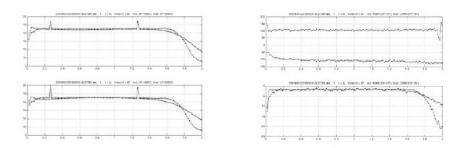


Figure 2. Comparison of the results of ABBC and NDAQ, source: 3C273B, one minute integration time; light line for ABBC and dark line for NDAQ. Left: auto spectrum of Seshan (top), Nanshan (bottom). Right: phase of cross spectrum (top), amplitude of cross spectrum (bottom)

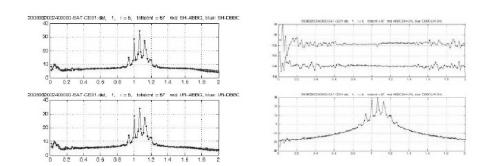


Figure 3. Comparison of the results of ABBC and NDAQ, source: CE-1 satellite one minute integration time; light line for ABBC and dark line for NDAQ. Left: auto spectrum of Seshan (top), Nanshan (bottom). Right: phase of cross spectrum (top), amplitude of cross spectrum (bottom)

# 3. The Correlator

The diagram of the 5-station correlator is shown in Fig. 4. It is based on XILINX Virtex-4 chips (XC4VSX35).

#### 4. The Future Plan

By the end of 2008 we will develop four NDAQ to install at four VLBI stations in China. The 5-station correlator will be extended to 10 stations with VSI.

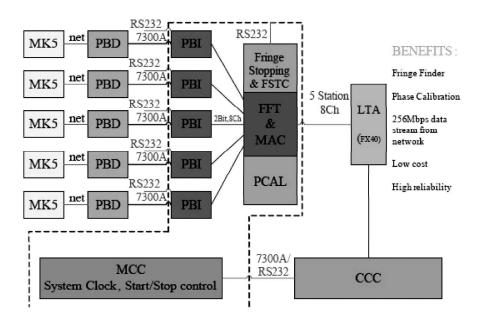


Figure 4. Diagram of 5-station correlator

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#### References

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