

The Digital Data Acquisition System for the Russian VLBI Network of New Generation

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Abstract

The system consists of several identical channels of 1024 MHz bandwidth each. In each channel, the RF band is frequency-translated to the intermediate frequency range 1 – 2 GHz. Each channel consists of two parts: the digitizer and Mark 5C recorder. The digitizer is placed on the antenna close to the corresponding Low-Noise Amplifier output and consists of the analog frequency converter, ADC, and a device for digital processing of the signals using FPGA. In the digitizer the subdigitization on frequency of 2048 MHz is used. For producing narrow-band channels and to interface with existing data acquisition systems, the polyphase filtering with FPGA can be used. Digital signals are re-quantized to 2-bits in the FPGA and are transferred to an input of Mark 5C through a fiber line. The breadboard model of the digitizer is being tested, and the data acquisition system is being designed.

1. Digital Data Acquisition System

A new generation national VLBI network based on small radiotelescopes is primarily intended for the daily monitoring of UT. Therefore it is not necessary to ensure compatibility with the existing “Quasar-KVO” VLBI network. But it is necessary to provide extremely high sensitivity of each receiver channel in order to ensure access to the maximum number of reference radio sources. The most obvious way to increase the sensitivity is to expand the bandwidth of the receiver channels from 16 – 32 MHz to 0.5 – 1 GHz with a corresponding increase of the data stream record rate. In addition, it is also necessary to expand the bandwidth of the intermediate frequencies (IF) to improve the accuracy of the VLBI measurements.

A significant expansion of the DAS channels’ bandwidth up to 1 GHz and a corresponding increase of the output data rate up to 4 Gb/s per channel can be achieved by using analog-to-digital conversion and digital signal processing directly in the IF range. Modern analog-to-digital converters (ADCs) can digitize IF signals and avoid a signal transfer to baseband using analog methods. The sampling frequency of such ADCs is able to achieve a few GHz, the number of bits reaches up to 10, and the input bandwidth reaches up to 5 GHz [1], [2], [3].

The new generation digital DAS developed at Institute of Applied Astronomy consists of a 10-channel RF/IF downconverter and four identical digital signal processing (DSP) units (Figure 1). **The RF/IF downconverter** converts input signal spectra from a multi-band radio irradiator of the radiotelescope (*C*, *X*, *S* and *Ku* bands) to the IF range of 1–2 GHz. Eight of ten channels of the RF/IF downconverter can be tuned in the wide frequency range of 3–14 GHz. There is no downconversion in the other two channels intended for S-band, because it can be directly digitized by ADC; but the signal is amplified and filtered. The downconverter receives the signals of five bands (*S*, *C – low*, *C – high*, *X*, *Ku*) in two polarizations (two channels for each band) simultaneously. Each DSP unit can be connected to the outputs of the RF/IF downconverter through an IF switch.

The DSP unit is the basis of the DAS and contains the following devices (Figure 2):

- ADC,
- FPGA,
- Clock oscillator,
- Demultiplexer of the ADC output signal,
- Flash RAM to store FPGA firmware,
- Microcontroller,
- Optical transmitters.

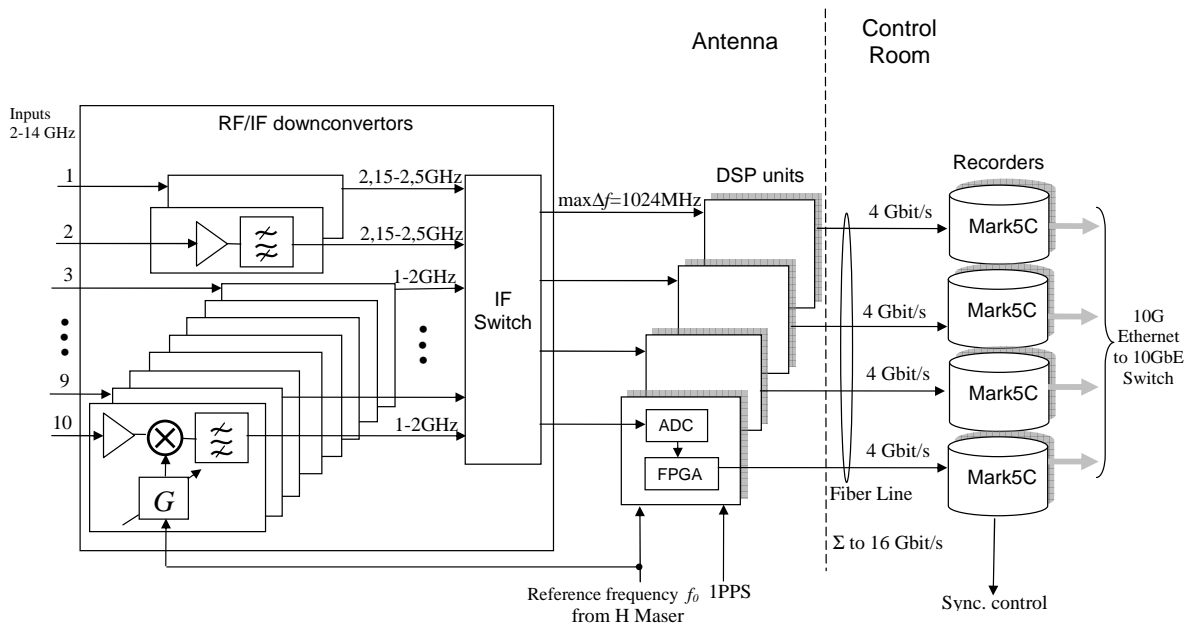


Figure 1. The Digital Data Acquisition System for the Russian VLBI-network of new generation.

It will be implemented as a single multilayer-printed circuit board (PCB).

The sampling rate of the ADC is 2048 MSamples/s. It corresponds to an IF bandwidth of 1024 MHz and a total output data stream rate of the ADC of about 20 Gb/s. It is necessary to decrease the sample arrival rate in order to transmit the stream into FPGA. This can be done by the demultiplexer at the ADC output. The demultiplexer 1 : 4 decreases the sample arrival rate to 512 MSamples/s. The use of the sampling frequency of 2048 MHz instead of 2000 MHz simplifies the coupling of the digital DAS with the existing data recording systems which usually use clock frequencies that are powers of 2 (e.g., 32 or 64 MHz in devices using VSI-H format [4]). Each DSP unit is synchronized by a hydrogen maser to ensure a long-term stability of the clock frequencies.

The FPGA performs the following operations: measurement of the rms level of the input signal, division of the fullband input signal into narrowband channels and converting it to the baseband (if necessary), calculation of the rms level of the narrowband channels, 2-bit quantization of the

output signals, generation of a test vector to check the transmission line and data recording system, formatting the output data in accordance with a data recording system interface, and sending them to the optical transmitters.

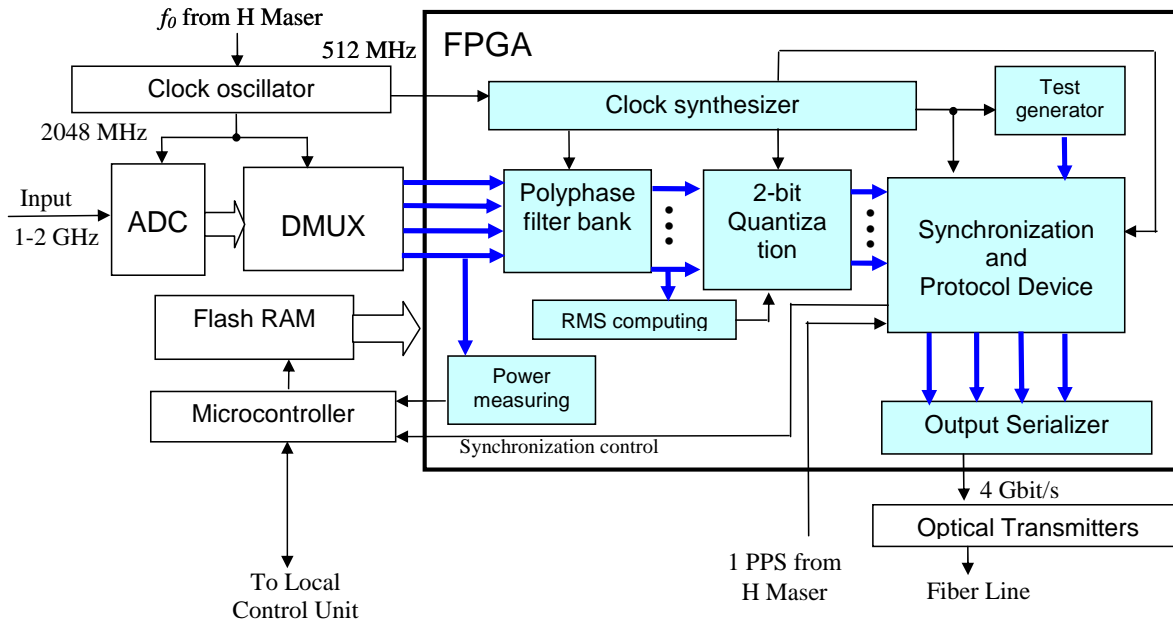


Figure 2. The DSP unit of the Digital Data Acquisition System.

The microcontroller provides the communication with the local control unit, execution of its commands, and loading of the appropriate firmware to the FPGA.

The previous DAS can be replaced by the DSP unit which is only one PCB. So the new digital DAS has lower weight and smaller size. That is why it can be mounted on the antenna. Output data streams are transmitted from the DAS to the data recording systems located in a control room.

The basic principles of the new generation DAS can be formulated as follows:

1. The DAS should be a modular system consisting of identical RF/IF downconverter channels and DSP units with frequency bandwidth of 1024 MHz.

The modular structure of the DAS is easily scalable and configurable for the required tasks.

2. Using undersampling.

Undersampling is a sampling technique that utilizes the aliasing signal caused by using a sampling frequency lower than the Nyquist frequency. In this technique the signal is sampled and simultaneously converted to low frequency [5], [6].

Undersampling allows the use of a sampling frequency of 2048 MHz to digitize IF signal of 1024 – 2048 MHz frequency range.

3. Using a fiber-optical communication line for the transmission of signals from the antenna to the control room.

As the DAS is located on the antenna, the signal is transmitted to the control room by a

fiber-optic line in digital form. It excludes any communication line influence on the signal.

4. Using an existing data recording system.

The DAS output data streams must be recorded with a data rate of 4 Gb/s per channel. This data rate is achievable by the Mark 5C recording system of Conduant Corp [7]. For each channel of the DAS, one Mark 5C is required.

5. Using a polyphase filter bank for dividing the fullband input signal into narrowband channels to work with previous DASs.

When the bandwidth of the DAS channels is 1024 MHz, the main processing operation is 2-bit quantizing of the input signal. No filtering is required in this case, which means that only a bit of computing resources of FPGA are used. There is an opportunity to carry out consistent observations by using the existing and digital DAS simultaneously. For this purpose the input 1024 MHz bandwidth of the digital DAS can be divided into narrowband channels.

The dividing into channels can be performed by a polyphase filter bank [6].

6. Supervision of the data streams.

The FPGA in each DSP unit measures the rms level of the input digital signal and the output channels. The measured levels are used for the calibration of the radio telescope, automatic setting of the optimal input signal level of the ADC, and determination of the quantizing threshold. Supervision of the amplitude-frequency characteristic, a phase calibration signal and an output 2-bit signal are distributed through each channel by the data recording system by making a short time trial recording just before an observation and analyzing it. The data recording system also verifies the transferred data for errors. The state of the equipment is written to the log-file in the local control unit during the observation and is then transmitted to the correlation center.

The DAS described above provides a flexible architecture consisting of identical channels. The new generation digital DAS allows a significant increase of the sensitivity of VLBI in comparison to the existing analog DAS. It gives the opportunity of using antennas of smaller diameter.

A prototype of the DSP unit (Figure 3) was made to check the basic principles. The prototype consists of evaluation boards of the following devices:

- 10-bit ADC (AT84AS008-EB),
- High-frequency demultiplexer 1:4 (AT84CS001-EB),
- FPGA XC5VFX70T (ML507),
- Optical transceiver AFCT-5710LZ.

The following tests have been made by using the prototype:

- Transmission of an internally generated test signal from ADC through demultiplexer to FPGA,
- Transfer of the test signal from one FPGA to another by fiber-optical line,
- Digitization of a signal from an external signal generator,
- Measuring of the input signal power.

The tests of the prototype provide the opportunity to implement the digital DAS with modern electronic components.

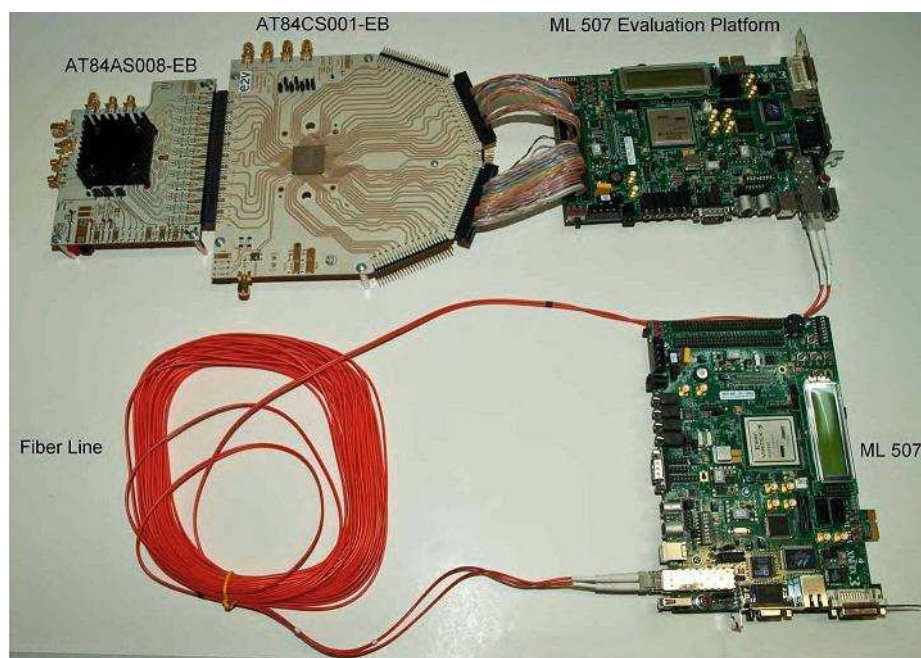


Figure 3. The prototype of the DSP unit of the Digital Data Acquisition System.

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