Current Development State of the Russian VLBI Broadband Acquisition System

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Abstract The Institute of Applied Astronomy is currently creating a new radio interferometer consisting of two 13-meter antennas. A Broadband Acquisition System (BRAS) was developed and manufactured to equip the antennas with modern digital backends. BRAS contains eight 512-MHz channels. Each channel has a separate 10G Ethernet fiber link for transmitting the output data. The data consist of 2-bit or 8-bit samples packed into VDIF frames. We are currenlty performing tests of two created systems and are developing a new version of BRAS with 1024 MHz channels.

Keywords BRAS, MDBE, DAS, FPGA, Quasar network

1 Introduction

IAA RAS is creating a new radio interferometer consisting of 13-meter antennas. The collecting area of the antennas is relatively small in comparison to most of the existing VLBI antennas. To compensate for the resulting sensitivity loss, it is necessary to significantly increase the bandwidth of the recorded signal. This cannot be done with the existing data acquisition system R1002M DAS, which is currently used at the observatories of the "Quasar" network. To equip the antennas with a modern digital backend, the Broadband Acquisition System (BRAS) was developed and manufactured at IAA RAS [1].

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2 Broadband Acquisition System

BRAS consists of eight identical channels of 512-MHz bandwidth each (Figure 1). The channels receive the signals in the intermediate frequency (IF) range from 1024 MHz to 1536 MHz. Eight-bit analog-to-digital converters (ADC), used in BRAS to digitize the in-

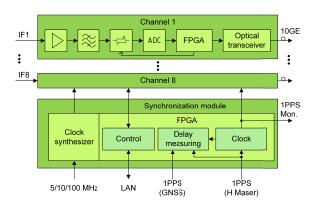


Fig. 1 Simplified structure of BRAS.

put signals, are clocked at 1024 MHz and have large enough input bandwidth to work in the third Nyquist zone. The 8-bit samples are processed by FPGA. The main purpose of FPGA is to pack the input samples into frames in the required format (VDIF) and with the corresponding timestamps, and to send the derived frames to the recording system through a 10 G Ethernet fiber-optic link. The output samples can be 8-bit or 2-bit. In the case of 2-bit data, FPGA measures the RMS level of the input signal and uses it as a threshold to requantize the signal to two bits. To provide time information, BRAS uses an internal clock synchronized to

an external 1PPS signal from an H-maser. Each VDIF frame has the timestamp information in its header.



Fig. 2 Photo of the Broadband Acquisition System BRAS.

BRAS has a flexible output data formatter allowing different output modes. It provides a selectable VDIF payload size in a wide range of possible values from 1000 to 8192 bytes allowing the use of Jumbo frames. By default, BRAS encapsulates the VDIF frames into pure Ethernet frames without any overhead; but it is also possible to add IP and UDP headers. In addition, one can change the transmission medium from fiber to copper by replacing the transceiver. Besides the abovementioned properties, FPGA performs several analysis features. It measures the input signal power with 0.25 second integration time. This data is used internally in the automatic gain control loop and is available in the control software. FPGA also collects 2-bit data statistics, which is useful for a quick analysis of the signal distribution and to detect strong signal distortions and interferences. Other useful features are the extraction of the phase calibration signal (PCAL) and the capture of the 1-microsecond input signal once per second. It gives rich possibilities for time and frequency domain analysis with software to evaluate the signal quality and system performance. Besides that, BRAS monitors the time difference between the internal 1PPS signal and any of the two 1PPS inputs. A BRAS prototype was successfully tested with real observations [2, 3]. Currently the system is ready for installation on the antennas (Figure 2). Key features of BRAS are summarized in Table 1.

Table 1 Key features of BRAS.

Number of channels	8
IF inputs	1024–1536 MHz
Channel bandwidth	512 MHz
ADC	8 bits, Fs=1024 MHz
Output samples width	2/8 bits
Total data rate	16/64 Gbps
Data frames format	VDIF
VDIF payload size	1000, 1024, 1280, 1600, 2000,,
	8000, 8192 bytes
Output interface	10G Ethernet, X2 transceiver,
	fiber/copper
Output headers modes	Pure Ethernet frame,
	Ethernet + IP,
	Ethernet + IP + UDP
Control interface	10/100 Ethernet
Sync signals	5/10/100 MHz
	1 PPS x2
Automatic gain control	For each channel, 31 dB
Analysis features	Signal power
	2-bit data statistics
	PCAL extraction
	Both 8 and 2-bit signal capture
	(1024 samples)
	Spectrum analysis of captured signal
	and extracted PCAL (implemented
	in software)
	1PPS int-ext delay monitoring
Telemetry	Power circuits current, temperature
	of PCBs and ADCs
Power consumption	75 W
Size	19" case, 483x314x242 mm (WxHxD)

3 Multipurpose Digital Backend (MDBE)

The development of BRAS gave us the necessary experience to design a more complex and advanced backend— Multipurpose Digital Backend (MDBE). MDBE is intended to upgrade the backends of the "Quasar" network antennas and to allow it to operate both in conventional downconverter mode for compatibility with the existing data acquisition system and in broadband channel mode. MDBE has two four-channel ADCs with 1024-MHz sampling frequency giving overall eight channels with 512-MHz bandwidth (Figure 3). By using the ADC interleaving mode, MDBE can combine adjacent channels and operate in a four-channel mode with 1024 MHz bandwidth per channel. A powerful FPGA with embedded dual-core ARM processor used in the MDBE can perform quite complex digital signal processing. Along with the remote firmware reload supported by MDBE, it allows

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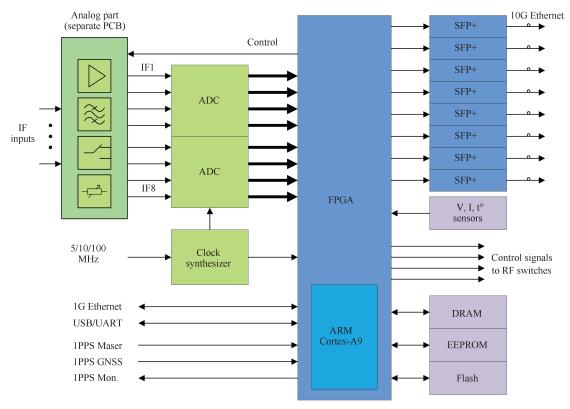


Fig. 3 Multipurpose Digital Backend structure.

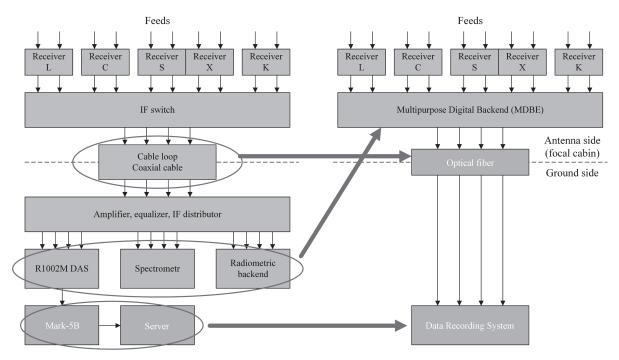


Fig. 4 Planned upgrade of the signal chain for RT-32 antennas.

to utilize the device for many radio astronomical tasks besides conventional VLBI applications. For example, spectrometer and radiometric backend modes are planned to be implemented. That means that the MDBE can combine all required backends into one device, greatly simplifying the signal chain structure (Figure 4). The MDBE will be located in the focal cabin of the antenna, which allows to eliminate long coaxial cables and auxiliary equipment used for signal transmission from the antenna to the control room and to replace it with fiber optic. Digital signals transmitted through fibers are insensitive to EMI, frequency response distortions, group delay variations, and so on. Using it can improve the quality of the VLBI data. The data recording system based on COTS components will be used to buffer the data [4]. It is also possible to copy data from the data recording system to Mark 5B for the case that the e-VLBI mode is not available. The MDBE is designed to be functionally compatible with the existing VLBI equipment, providing interoperability in international observations.

4 Conclusions

The Broadband Acquisition System for VLBI observations with 512-MHz bandwidth per channel was created. The prototype of BRAS was tested with real observations and first fringes were obtained. Currently the system is ready for installation on the new 13-meter antennas. In order to upgrade the existing equipment, to unify the instrumentation on all antennas of IAA RAS, and to provide a full set of modern radio astronomical backends, the development of the new Multipurpose Digital Backend was recently begun. The MDBE supports 1024-MHz bandwidth, remotely firmware reloading, and provides powerful computing resources.

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