DBBC3: An EVN and VGOS All-inclusive VLBI System

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Abstract The DBBC3 project is rapidly evolving in all its main components. The hardware of the astronomical L version is complete in the main parts, and the VGOS H version is progressing as planned. The DBBR receiver is under test and is expected to be placed in the antenna in the next few months. A first implementation of the L version includes the ability to support the VGOS requirements. A detailed status of the different structural parts is described, ranging from the front-end to the 32 Gbps disk and network capability, expandable up to 64 Gbps.

Keywords Backend, DBBC

1 Introduction

The development of the DBBC started in 2004, after in previous few years ad-hoc laboratory experiments and experiments with real sky signals had demonstrated that it would be possible to emulate with fully digital equipment the entire functionality of the Mark IV VLBI analog terminal. In the digital process, the signal available as IF from the receiver is immediately converted to a digital representation. This complete digital process could not be fully implemented at a reasonable cost, and moreover at that time it was a technical challenge due to the wideband and the high frequencies involved. During the first decade of 2000, with progressive improvements, the DBBC project evolved to cope with an input bandwidth of up to 4×1 GHz. The first DBBC version (DBBC1; 2004–2008) was a backwards compatible replacement of the existing VLBI terminal, while with the DBBC2 (2007 to date), additional observing modes, which did not exist in the analog backend, became available. The enhanced version of the DBBC2 for VGOS, the DBBC2010 (2009 to date), is compatible with the proposed VGOS observing, provided that an appropriate down-conversion of the broadband is realized in the analog domain. With new wideband receivers, the demand for backends which can handle bandwidths of several GHz has arisen. So both the new VGOS network and the EVN have been increasing their maximum data rate demand from a maximum of 1 Gbps with the Mark IV analog backend to something ranging between 32 and 64 Gbps. In particular for the EVN and the preparation for receivers and IF systems which will deliver up to 4 GHz (and later more) bandwidth to the backends, it was felt necessary to develop a system which can process an instantaneous bandwidth of 4 GHz per polarization as a minimum. The resulting output data rate for a dual polarization receiver should be at least 32 Gbps, with the option of 64 Gbps for a 4 IF system. Such a backend is the intermediate goal of the DBBC3 project. The specifications of VGOS define a set of features of the receiving/backend system to achieve the goal of greatly improved geodetic measurement precision. The telescopes will operate in a single broadband ranging from 2 to 14 GHz observing in dual linear polarization. Inside this frequency range a subset of four 1024 MHz wide pieces will be selected, in both polarizations. It is worth noting that then the actual selected input data rate will be equivalent in both EVN and VGOS. The wideband of the new VGOS network will realize bandwidth synthesis (phase slopes fitted over a wide frequency range) for a much wider portion of the spec-

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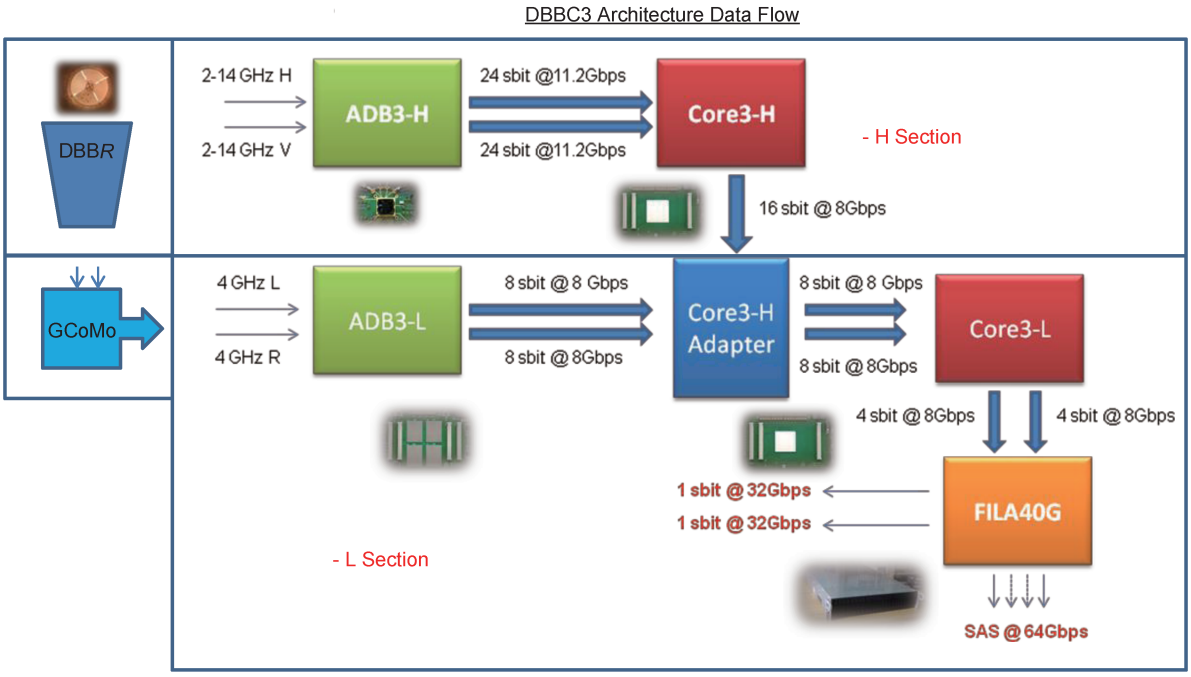

Fig. 1 General structure of the DBBC3.

trum than is possible with the present system. Such a wide input band could also be of great interest for astronomy because of the significant increase in sensitivity. Being able to process an entire 14 GHz-wide piece of band could be a quantum leap in digital radioastronomy data acquisition. This goal is very ambitious, and its implementation in a radio astronomy backend would be a novelty. To digitally sample and process the whole 14 GHz wideband or a number of sub-bands thereof is the final goal for the DBBC3 project.

2 DBBC3 Structure

The DBBC3 system needs to meet some compulsory requirements: backwards compatibility with the existing backends of the previous generations and the ability to realize the new functionality in the very wide band. It should also be able to accomplish all the required functionalities, for the planned EVN goals (minimum 2×4 GHz bandwidth) and VGOS (2×14 GHz bandwidth). Moreover, as many stations are active in both networks, a single system is mandatory, and flexibility is a requirement due to the different radio telescopes and their dissimilar receivers and IF systems in terms of their numbers and types of IFs. To be compatible with the existing systems, the new hardware needs to be mechanically and electrically level-compatible. This aspect is useful because existing DBBC terminals in the field could be upgraded to meet the new performance requirements by replacing the necessary parts. Components of the DBBC3 can be inserted into existing DBBC2 and DBBC2010 backends to augment their performance with additional functionalities.

The much higher performance of the new backends requires new hardware parts, to be supported by new firmware able to perform new functionality, that are a challenge for data volume and rate. A clear development path has been laid out to minimize the risk in the project. In a first step, a DBBC3-L will be developed which can be seen as a fully qualified 4 GHz DBBC and, at the same time, will allow us to study how best to achieve the final goal of a 14 GHz DDBC3-H. The first step is able to support both modes, EVN and VGOS, even if in this last case the input band is divided into four continuous progressive portions 4 GHz wide, up to 16 GHz.

The main features of the DBBC3-L system are:

- Maximum number of wide input IFs: four per polarization
- Instantaneous bandwidth in each IF: 4 GHz
- Sampling representation: 10 bit
- Processing capability N×5 TMACS (multiplication-accumulations per second), with N being the number of processing nodes
- Output data rate: maximum 64 Gbps
- Compatibility with the existing DBBC

The main features of the DBBC3-H system are:

- Maximum number of wide input IFs: four per polarization
- Instantaneous bandwidth in each IF: 14 GHz
- Sampling representation: 8 bit
- Processing capability N×5 TMACS
- Output data rate: maximum 896 Gbps
- Compatibility with the existing DBBC

This paper mainly describes the DBBC3-L version which is being specifically developed for the EVN network and is supported by RadioNet3. As already mentioned, this version will also be used in the first VGOS implementation. Figure 1 shows the overall structure of the DBBC3 including the data flow of both -L and -H.

The structure of the system is straightforward. Four IFs 4 GHz wide are sampled with 10-bit representation. This data is then transferred to one or more dedicated processing nodes, each with its own single element identity and functionality. The processors then extract from the digital data streams portions of the band (with digitally tunable mixers or fixed filters) and produce as VLBI-compatible output VDIF packets. The last element of the chain is the FILA40G subunit, whose function is to condense the data onto single optical fibers at 40 Gbps data rate and to handle the data at the network packet level. A dedicated version, the FILA40G-ST, will in addition have storage capabilities.

3 DBBR – Digital Broadband Receiver

The first unit mainly devoted to VGOS is the broadband receiver. The feed is coming from a deeply modified original project for telecommunication and renamed as “quad ridge in resonant chamber”. This is because having to cool it down at cryogenic temperatures, the performance is strongly influenced by the vacuum chamber and related shields. So it appeared convenient to have included as an active part the Dewar mechanics and to use it as an advantage more than to endure it as a side effect. The main characteristics of the DBBR are:

- Dual linear polarization
- 1 LNA per polarization
- Full range 1–16 GHz
- Radiation pattern versus frequency optimized for 3–14 GHz: 40–20 degrees @ −3dB
- Antenna factor versus frequency optimized for 3–14 GHz: 33–40 dB/m
- Optimized for cryogenic use (Dewar is active part)
- Entirely in copper
- Integration of custom cryogenic filters into the antenna body

The receiver is extremely compact and well-suited for 12-m class antennas. Its first use will be with the Noto antenna, where it will be adapted using a tertiary mirror.

4 GCoMo – Giga Conditioning Module

In a standard DBBC3 system, there could be from one to four units, available in more flavors with the capability of supporting a selection of four different frequency ranges: A (0–4 GHz), B (4–8 GHz), C (8–12 GHz), and D (12–16 GHz). For each range, the down-converted and the purely conditioned version will be available. This could help to simplify the receivers’ connections to the system. In the first VGOS implementation, this unit will allow access to the entire input range to be used with the ADB3-L samplers. Features of this unit are:

- Input: in real mode, four pre-filtered 4 GHz Nyquist bands; in complex mode, two pre-filtered 8 GHz bands
- Total power detectors independent in all the Nyquist zones
- Modular construction: any zone can be included
- Power level control in agc and manual mode
- Compatibility with the existing DBBC

5 ADB3-L Sampler

The massive 4 GHz sampling is performed by state of the art sampler chips. An extensive analysis is under way to determine the phase performance of those devices, as the interferometric use calls for high absolute phase stability and low temporal jitter. An alternative general method to increase the bandwidth is to make use of complex samples. Two channels in quadrature are sampled at a clock frequency equal to the full instantaneous bandwidth. A single ADB3-L has onboard four complete samplers, with the possibility of arranging them for a variety of functionalities, single and multiple, real or complex. Indeed, for example in real mode, the four samplers can be fed with a single input signal for the full 4 GHz functionality, so that they can be fed with two signals of 2 GHz instantaneous bandwidth each, or finally with four signals of 1 GHz bandwidth each. Sampled data are transferred to the processing units at a data rate of 80 Gbps for each ADB3-L board. The main features are:

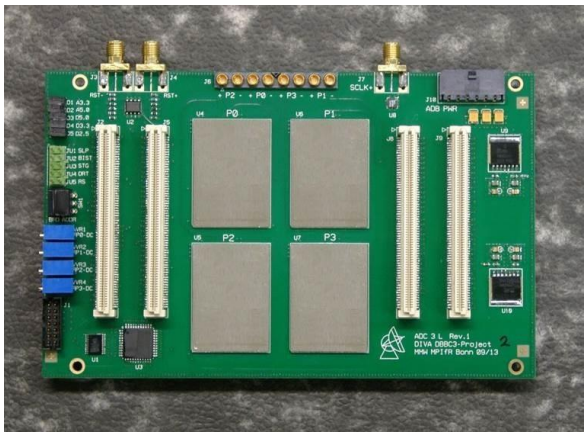

Fig. 2 ADB3-L board.

- Number of IFs: one to four
- Equivalent Sample Rate for full IF: 8 GSps
- Instantaneous bandwidth: 4 GHz
- Sampling representation: 10 bit
- Real/Complex Sampling
- Compatibility with existing DBBC

Figure 2 shows an ADB3-L board.

6 CORE3-L Processing Node

Data coming from the ADB3-L sampler board are routed to the processing node CORE3 using the lanes of the high speed input bus. This board is able to process data in different ways: DSC (Direct Sampling Conversion), DDC (Digital Down Converter), and PFB (Polyphase Filter Bank) functionalities. Additional capabilities will be spectroscopic and polarimetry observations. From the pool of channels, a subset is selected according to the desired output data rate defined by the observer or allowed by the recording or network media. The data is output through the high speed output bus. Additional input and output connections are available to maintain the compatibility with the DBBC2 stack. The large DSP resources available in the FPGA chosen for the CORE3-L allow digital filters in the class of 100 dB in/out band rejection. This feature is required for the expected presence of large RFI signals in the very wide input band. This very strong discrimination together with the tuning ability should be appropriate to obtain useful down-converted and clean pieces of the observed band. As an alternative input, the board will be able to receive data packets from a block of ADB3-H/CORE3-H units to be routed to the rest of the system for additional data processing. The functionality of the FILA10G used in the DBBC2 will be integrated in this unit for multiple 10G data I/O. In particular, this method is the output connection for the FILA40G unit. Figure 3 shows a

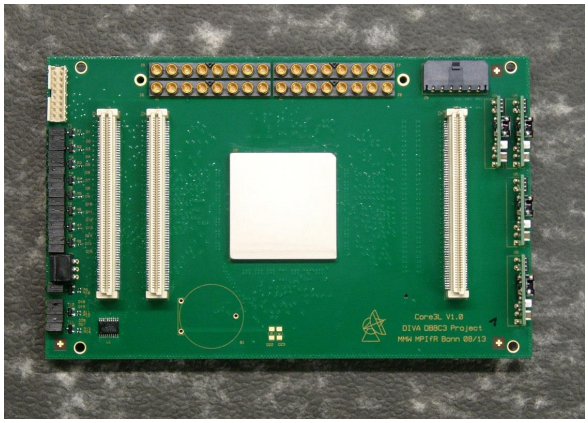

Fig. 3 CORE3-L board.

photo of the Core3-L board. The following list gives the main performance features:

- Number of I/O: maximum of 40 serial links, 12.5 Gbps
- Number of Output: maximum of 32 serial links, 11.2 Gbps
- Input Sampling Representation: 8–10 bit
- Processing capability: maximum of three TMACS
- Processing capability: WB-DDC, WB-PFB, WB-DSC
- Output: VDIF 10GE packets
- Compatibility with existing DBBC

7 FILA40G Network and Buffering Node

Data from the converted bands are finally transferred to the network controller FILA40G as multiple 10GE connections. The number of connections is then accumulated into a 40GE data stream to be transferred to the final destination points. Such final points could be recorders, nodes of VLBI correlators, or a buffer cloud. In addition to the 40G network capability, the FILA40G unit will be able to manipulate the data packets in order to perform functionalities such as corner-turning, pulsar-gating, packet filtering and routing, burst mode accumulation, and other functionalities that could be required at the packet level as soon as the VLBI methods evolve. In addition a dedicated version will be provided which can include storage elements for data buffering and recording. The general features are:

- 8 x 10GE Inputs
- 2 x 40GE Output
- Optional disk storage
- Expected recording rate of 32 Gbps
- Compatibilty with Mark 6 disk packs/chassis being investigated
- Stream aggregation
- Format conversion/VDIF threading
- Packet filtering
- Pulsar gating
- Timekeeping via NTP and/or GPS module
- Propagation of UTC to other connected devices via DBBC Local Network (DLN)

The available 10G skills are:

- Mark 5B up to 4 Gbps (native is 2 Gbps)
- VDIF Single Thread up to 8 Gbps
- VDIF Multiple Threads up to 8 Gbps
- RAW (no headers) up to 8 Gbps
- Threads can be fed by a selection of data channels eventually corner-turned
- The 10G Ethernet ports are independent in the destination address in VDIF-ST and Mark 5B
- The 10G Ethernet ports in multi-thread mode support an independent block of destination addresses coupled with the thread content selection
- Decimation and bit-mask are selectable at this level

Figure 4 shows a view of the FILA40G.

Fig. 4 FILA40G.

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