A New Generation of Platforms for CDAS

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Abstract A new platform was finished by the end of 2013. It contained two Xilinx K7 FPGAs for data processing, in addition to the capability of supporting two channels that each sample 512 MHz bandwidth or a single channel that samples 1024 MHz bandwidth. Compared with the previous platform, which consists of four Xilinx V4 FPGAs, the new one not only updates the key chips for DSP but also adds two 10-Gigabit Ethernet SFP+ ports for data transmission. The new platform also improves the performance and lowers the cost.

Keywords Backend, platform, CDAS

1 Introduction

With the development of VLSI technology, the capacity and performance of the FPGAs are growing exponentially. Therefore, we can achieve more and more complex algorithms in one chip.

With the previous platform used in CDAS, each module could sample 512 MHz bandwidth and convert it with four BBCs using a DDC algorithm with four Xilinx Virtex4 LX series FPGAs. As the CDAS has the capability of four input IF channels and 16 output BBCs, more than four modules are needed.

In contrast, with the new platform, one module has the capability of using dual channels to sample 512 MHz bandwidth apiece or using one channel for 1024 MHz bandwidth sampling. Compared with the previous platform, it not only updates the key chips from Xilinx Virtex4 series FPGAs to Kintex7 series FPGAs for DSP but also adds two 10-Gigabit Ethernet SFP+ ports for data transmission. The new platform also improves the performance and lowers the cost. It can deal with two input IF channels and produce output with at least eight BBCs using one chip. Furthermore, the output data can be recorded by commercial disk array server with the 10-Gigabit Ethernet. The new platform will be used in CDAS2.

After that, another platform, which will be implemented with a 5-Gsps ADC, will be put on the agenda in the near future.

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2 The New Platform

As shown in Figure 1, the new platform consists of one ADC for sampling, two FPGAs for data processing, and two SFP+ ports for data transfer. PPC and other peripherals make the system run in standalone mode.

Platform characteristics:

- Dual channel ADC with 8-bit resolution
- 1 Gsps sampling rate per channel
- 2 Gsps in Interlaced Mode
- One Xilinx Virtex4 FX for control
- Two Xilinx Kintex7 for data processing
- Two SPF+ for 10-Gigabit Ethernet
- One RTC for system time

The FPGA1 is the master chip with two 10-Gigabit Ethernet ports attached. The FPGA2 is a servant chip, and there is no high speed port for data output. If the

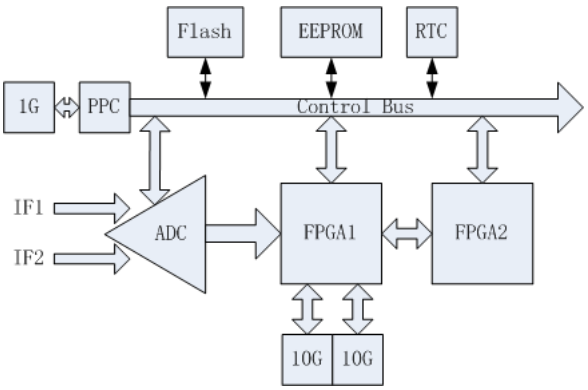

Fig. 1 The construction of the new platform.

Fig. 2 The module of the new platform.

master chip can meet the requirements for data processing, the other chip can be omitted. The control system is set up by PowerPC405, which is embedded in Xilinx Virtex4 FX series FPGAs. With peripherals such as flash, EEPROM, RTC, and Gigabit Ethernet attached, it can work in standalone mode.

The FPGAs used by the new platform can be selected from the Xilinx Kintex7 series, whose package is FFG901. Table 1 shows the differences between Xilinx Virtex4 LX160, which was used in the previous platform, and Xilinx Kintex7 480T, which can be used in the new platform for the same amount of resources. Compared to the Virtex4 LX160, Kintex7 480T has more than ten times as many DSP slices and six times as many RAMs, which are more useful for the complex algorithms.

Table 1 Virtex4 LX160 and Kintex7 480T Resources.

Parameters		XC4VLX160 [1] -10FF1148C	XC7K480T [2] -1FF901C
Logic Cells		152,064	477,760
CLB	Distrubuted RAM (Kb)	1,056	6,788
	DSP Slices	96	1,920
Block RAM	18 Kb	288	1,910
	36 Kb	—	955
	Max	5,184	34,380
DCMs/CMTs		12	8
PCIe		–	1
GTXs		–	28
XADC		–	1
Total I/O banks		17	8
MAX User I/O		960	380

3 PFB Version of CDAS2

With the new platform, a PFB version of CDAS2 is undergoing testing now. As Figure 3 shows, it consists of one module with only the master Kintex7 FPGA on it.

CDAS2 now works in two modes:

- 512 MHz Dual IF Mode:
  For each IF, it has
  - 512 MHz bandwidth input
  - 16 output channels
  - 32 MHz bandwidth for each output channel
- 1024 MHz Single IF Mode: 16 channels x 64 MHz baseband output
  - 1024 MHz bandwidth input
  - 16 output channels
  - 64 MHz bandwidth for each output channel

Fig. 3 PFB version of CDAS2.

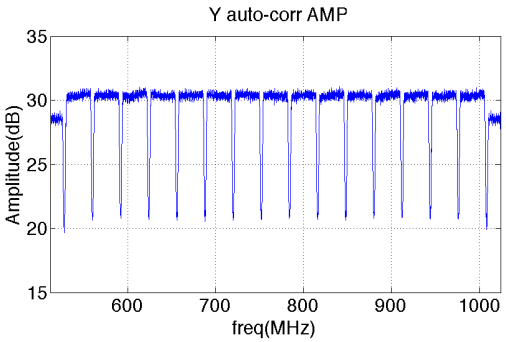

Fig. 4 The bandpass of PFB.

Due to the PFB algorithms, the first channel in each mode is different from the others. Figure 4 shows the characteristics of the 512 MHz (512–1024 MHz) bandwidth.

4 Future Plan

In the near future, a 5-Gsps ADC platform will be applied. This platform consists of two modules—an ADC module (Figure 5) and a DSP module (Figure 6). These two modules are connected by the backplane.

- ADC module
  - Quad channel ADC with 10-bit resolution
  - 1.25 Gsps sampling rate in four-channel mode
  - 2.5 Gsps sampling rate in two-channel mode
  - 5 Gsps sampling rate in one-channel mode
- DSP module
  - ARM7 for control
  - Xilinx Kintex7 480T for data processing
  - 6 SPF+ for TenGiga Ethernet
  - 8 GB DDR3
  - 1 Gsps DAC output

After connecting these two modules, it can be a new backend.

For this backend in the future:

- Wider bandwidth can be processed in one chip
- Original sampling data can be transmitted over the network
- Intermediate results can be temporarily stored in DDR3
- DAC (analog) output will be possible.

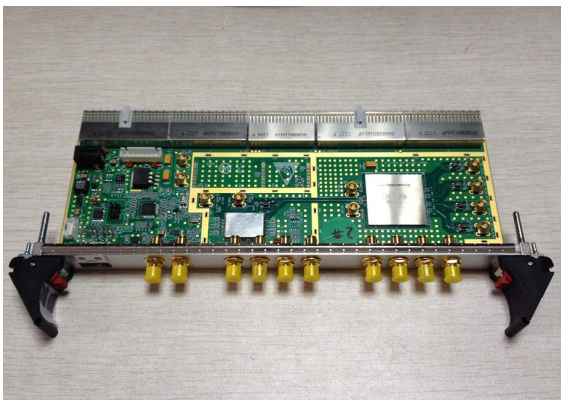

Fig. 5 5-Gsps ADC module.

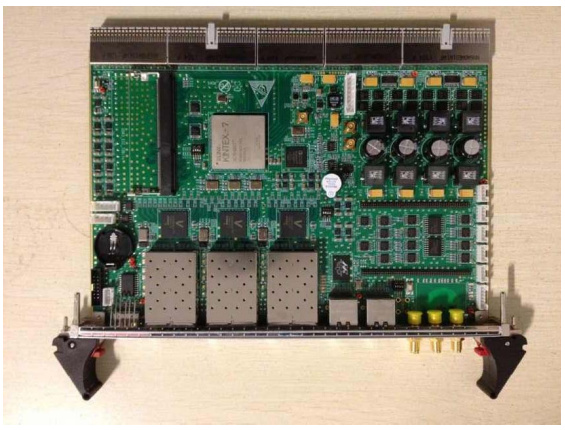

Fig. 6 5-Gsps DSP module.

Table 2 Comparison among the three platforms.

Platform	CDAS	CDAS2	Future
Number of input IFs	1	2	4
Sample mode [CH@Msps]	1 @ 1024	2 @ 1024 1 @ 2048	4 @ 1024 2 @ 2048 1 @ 4096
FPGA series	4 × Virtex4 LX160	2 × Kintex7 480T	1 × Kintex7 480T
Interface	VSI	2 × 10-GigE	6 × 10-GigE
Memory	No	No	8 GB DDR3
DAC	No	No	Yes
Planned schedule	complete	2014	2015

5 Summary

Comparing the three platforms described above, Table 2 shows the differences among the three platforms.

We plan to test the CDAS2 in our VLBI stations this year and prepare the 5-Gsps platform for the future.

References

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