

VLBI Data Playback in FPGA

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Abstract The correlator as the VLBI core data pre-processor is a complex, high-speed, and real-time signal processing system. We have successfully used it to process VLBI observations of the Chang'E mission. For the VLBI hardware correlator (HCORR), the original VLBI data of the stations must be read and pre-processed before correlation. We focus on VLBI data playback at the correlator for Chang'E-3 data of 2013. The VLBI playback system uses a 1-Gb Ethernet network to transmit station data and design some pre-processing method such as data correction and data decoding specific to VLBI data. The Chang'E-3 results show that the system is able to playback VLBI data in real-time, while ensuring data validity and meeting the requirements of the VLBI observations. We conclude with an outlook on future research plans for the VLBI data playback system.

Keywords VLBI, correlator, playback, pre-processing

1 Introduction

Very Long Baseline Interferometry (VLBI) is an important radio astronomy technique (Zheng) that is widely used for high-precision measurements of deep-space probes. We have successfully used VLBI to perform observations for the Chang'E mission. In China, the VLBI infrastructure is comprised of the VLBI stations, data pre-processing, correlator, post-correlator, SKD, orbit, location, and so on. The

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correlator is the core device of the VLBI data pre-processing unit able to calculate important parameters such as the delay, delay rate, correlation amplitude, and interferometric phase. The correlator can be divided into hardware correlator and software correlator. High-speed, large-scale correlators are mostly hardware correlators, so the hardware correlator is very important. The hardware correlator and its data playback system use a special hardware platform such as a Field Programmable Gate Array (FPGA). The rapid development and optimized mutual integration of the FPGA with high-speed networks made miniaturization possible for a low-power, high-speed, and real-time VLBI data playback system.

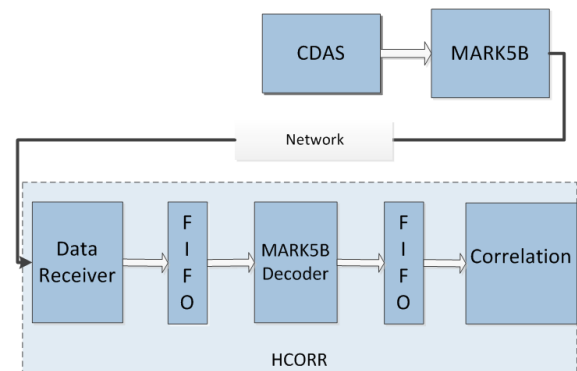


Fig. 1 Diagram of the VLBI data system.

Figure 1 shows the VLBI data system. The system uses the Chinese Data Acquisition System (CDAS) to collect original VLBI data and the Mark 5B system to record and playback the observed data. The HCORR shall receives the VLBI data from the Mark 5B system via Internet and calculates the delay, delay rate, corre-

lation amplitude, and interferometric phase with proper control parameters given from the correlator control computer, and then transmits the correlation results to the post-correlator. HCORR uses FPGA as the hardware platform and mainly includes the data playback system and correlation module. The VLBI data playback of the correlator includes the network control data playback module, the data receiver, and the cache module. In December 2013, the VLBI system was used in the Chang'E-3 mission. We used the HCORR real-time mode and post-correlation and the results proved that the requirements of the Chang'E-3 mission can be met.

2 System Description

For the Chang'E-3 mission, the specifications for the correlator are the following (Zhang, 2012):

- Number of stations: four
- Bandwidth per station: 64 MHz
- Input resolution (max): 1–32 bits
- Correlation points: 1024 or 2048
- Data input format: Mark 5B

The hardware correlator design can reach 128-MHz bandwidth per station in real-time data processing. Figure 2 shows the conceptual configuration of the hardware correlator system. There can be four observation stations, e.g., Beijing (BJ), Kunming (KM), Urumchi (UR), Shanghai (SH), or any other station that can participate in the VLBI observations. The stations' data is transmitted through the network and is recorded to the data cache and distributed components (DDU). One DDU corresponds to one station. Finally, the DDUs distribute the data to the correlator across the 1-Gb Ethernet network. The dotted line encircles the hardware correlator modules. The hardware correlator VLBI data playback interface module (VSIDOM) receives the VLBI data from the DDU system, pre-processes the data w.r.t. the data format, and then dumps the pre-processed data into the correlation system. The correlation system is the core algorithm of data server, which is used to calculate the correlation of stations. The correlation system includes the Fourier transformation and cross-multiplication module (FFT and MAC) as well as the Long Time Accumulation module (LTA). The Computer Control (CCC) is the correlator and operation computer, which

is used to send proper control parameters and to save the correlation data as a structured file system for the post-correlator.

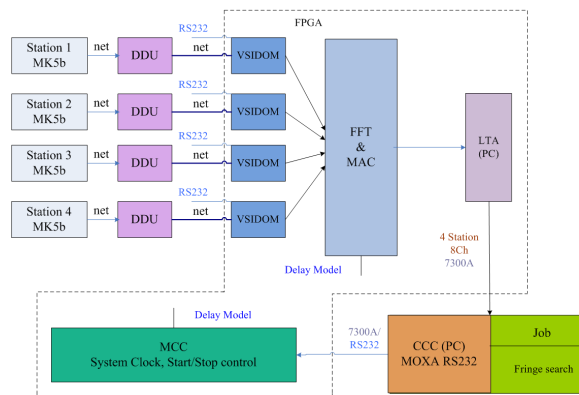


Fig. 2 Diagram of the HCORR system (Xu, 2006).

The VLBI data playback system is an indispensable part of the hardware correlator system. It reads station data and pre-processes raw VLBI observation data needed for the correlation system. The overall scheme for the VLBI data playback of HCORR is shown in Figure 3 for one station (VSIDOM).

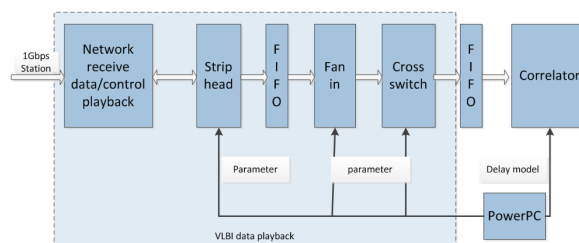


Fig. 3 The VLBI data playback of the HCORR.

2.1 Network Module

The network module has a 1-Gb Ethernet input port to connect to the data cache and distributed components (DDU) for data playback. It allows the user to read data via the 1-Gb Ethernet interface and to write data to registers for the next module. It will feedback full mark to control the DDU data playback continue. Data are transmitted from the stations in Mark-5B-

formatted UDP packets. The cache space of the hardware correlator in real-time mode is limited because of the use of FPGA. When all stations' data is synchronized all the time, just process continuously. When checked, if some stations data reach synchronization time but other stations do not, then wait for the feedback client to stop sending data, otherwise it will cause data overflow. When all stations are synchronized, tell the client to send data continuously, then recorded data can be processed validly. In this network interface data are transmitting from the stations in Mark5B-formatted UDP packets, and improving response mode, to ensure that the data transmission is more reliable. The network interface module of the VLBI data playback system (VSIDOM) and the data playback module in DDU form a complete set of network transmission system, using the client/server mode, data playback module in DDU send part for the client network, network interface module of VSIDOM for the server. When the DDU through Ethernet received data from the observatory stations, began to prepare to send data to the VLBI data playback system. There are several steps:

1. Connection to the Ethernet, the client sends an ARP request frame to ask the server MAC address, after the server receives an ARP request frame and send ARP reply frame, if client receives an ARP reply from the server then start data transfer.
2. The client sends a packet and waits for feedback data. At the same time, the timeout timer is started. If received server response frame, continues to send the next frame, timeout timer resets at the same time, if the timeout timer more than set threshold, argues that the UDP packet loss, client resends just the frame data.
3. The server receives packets from the determined client. When the FPGA pre-process data rate is less than the capacity of client send data, not send reply to the client server network. If the recorded data can be processed continuously as per real time data, then send the reply packet to client.

2.2 Parameters

The VLBI data pre-processing parameters are provided by the CCC. The FPGA communicate with the CCC through the Peripheral Component Interface (PCI) bus which will drive by the PCI drive module. The PCI rate

can reach 264 MB/s, which can meet the real-time data playback mode. The VLBI data pre-processing parameters adhere to a specific format and include:

- Strip head parameters: correlation start time and end time, frame number.
- Fan in parameters: the number of valid bit streams.
- Cross switch parameters: each bit need in position.
- And other parameters such as system reset, system start, FFT start and so on.

2.3 Pre-process Module

The main specification of the pre-processing interface module was described in Figure 3. The infrastructure of course provides the FPGA top-file, connecting three modules includes the strip head module, the fan in module, and the cross switch module. The pre-processing module has the capability to frame header parsing, CRC checking, get the raw and valid data, arrange data in the required format, send the frame header information and error number to the correlator control and operation computer which is used to check playback time synchronization. As normally, there are four stations playback and process at the same time, but at some special status, fewer than four station, then need do some special processing. There are several situations:

- Before the start of the HCORR system. To shield the station which cannot playback VLBI data, and pad with zeros as the station data.
- In running. If stop data playback, there will timeout overflow and give up the scan data all station. If cannot restore at a long time, then need to stop the HCORR system, turn off the station, restart HCORR system.

The function of the strip head module is strip frame head and get the data. Mark 5B format data has frame header and data field. A frame size is 10016 bytes includes 16 bytes frame head and 10000 bytes data. From the frame header we can get synchronous word such as ABADDEED, can get frame number within seconds, BCD time stamps and CRC code. The mainly functions of strip head module are:

- Determine synchronous word. In normally, ever frame set synchronous word to constant ABAD-

DEED, only find the constant means the frame is start.

- BCD time stamps. The time stamp in the header also is used to determine the data playback start or stop. As the hardware correlation actions must be required to synchronize timing between the stations. When the start time is reached, the correlator requests the DDU to send data and process recorded data. By comparing the time stamp in the header with stop time from CCC, if the same then the data processing stop.
- CRC. Calculate synchronous word, custom information, seconds time frame number, BCD code calculation to a check code, comparing with the CRC of frame header, if the same, can be concluded that the frame header information is correct, so as to start recording data.
- Finally combined the time stamps (48 bit) from frame header and error number (16 bit) which count the error frame into two 32-bit data, send to the CCC system.

Fan in module according to the number of effective bit-stream which given from the CCC, recovering data word from Mark 5B recording equipment each time sampling to get valid data bits, such as effective for 1 bit, need 32 times to recover a 32-bit data and one bit for each time, from low to high, each bit combine with 31-bit zeros to 32-bit data, will rearrange data in chronological order, and transfer to the cross selection module. Cross switch module shall cross the restoration bit-stream with cross parameters given from the CCC to the new order data, and finally record data to the buffer.

3 Conclusions

The data is Chang'E-3 (Chinese Lunar Exploration Program) observations of lunar flight information on December 13, 2013. There are four observation stations: Beijing (BJ), Kunming (KM), Urumchi (UR), and Tianma (TM). The HCORR can support the recording and playing back speed is 256 Mbps. Figure 4 shows the time delay analysis of HCORR for the collected satellite data. Each point represents a processing unit (scan), is a satellite data point, each scan is 5-s data. Figure 4 is the difference between

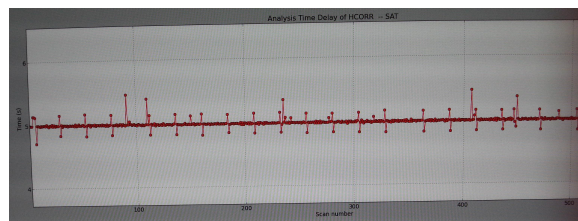


Fig. 4 Time delay analysis of HCORR.

the two scan begin processing time. From the figure you can see that the time delay is 4 s to 6 s, normal for 5 s. When more than 5 s is because the process data rate is less than the capacity of playback real-time data, and less than 5 s because is the processing of the correlator faster than real-time. The result was checked to make sure the VLBI data playback system can meet the needs of the real-time playback. Figure 5 is the result of real-time correlator, while the left six graphs present the correlation delay and the right six graphs show the correlation delay rate. There are four stations (BJ, KM, UR, and TM). BK means BJ and KM, BU means BJ and UR, BT means BJ and TM, KU means KM and UR, KT means KM and TM, UT means UR and TM. Using the real-time mode of

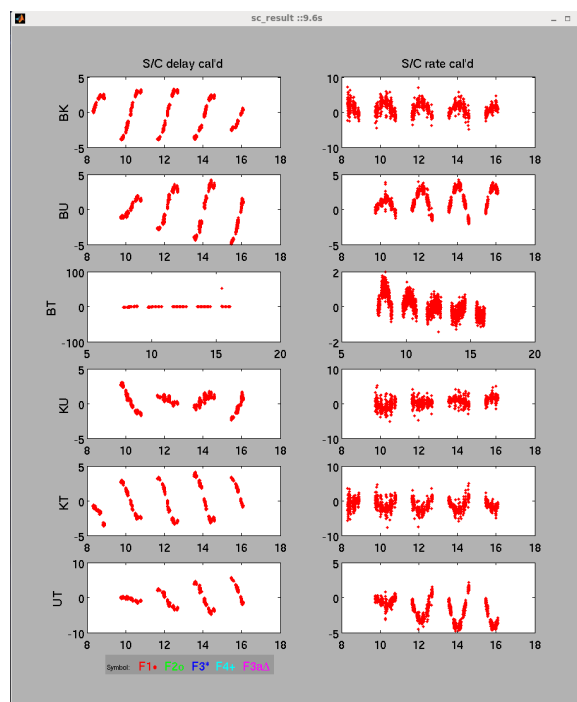


Fig. 5 Delay and delay rate.

HCORR and post-correlator, we can handle the result of the correlation processing at the same time.

- VLBI data input interface: 10-Gb Ethernet
- CCC control interface: 1-Gb Ethernet

4 Future Plans

The SHAO participated in the Uniboard development with JIVE as a member of international consortium. So, in the near future our group will port the whole system to Uniboard for speed improvement and supporting more modes. The next generation hardware correlator design goal are (Hargreaves, 2011):

- Number of stations: four
- Sample rate per station: 2 Gbps
- Input resolution (max): 1–32 bits
- Correlation points: 1024 or 2048
- Data Input Format: Mark 5B

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