Hardware Correlator Development at SHAO

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Abstract The CE-1 and CE-2 hardware correlators have been used for the Chinese Chang'E-1 and Chang'E-2 missions. Recently, the CE-3 hardware correlator has been successfully used for the Chang'E-3 mission. This paper presents the development of the hardware correlator at SHAO and some results of the Chang'E-3 mission.

Keywords Hardware correlator, FPGA, Chang'E

1 Introduction

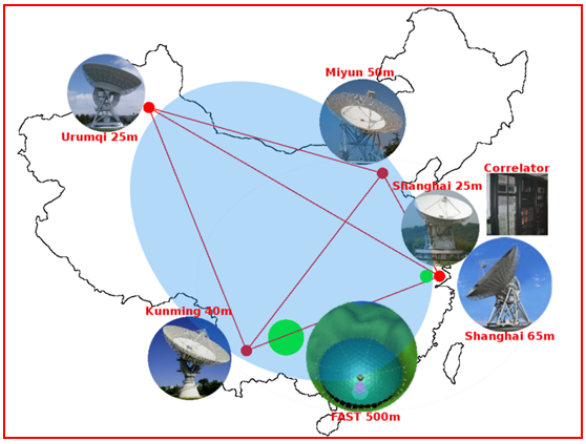

Fig. 1 Chinese VLBI Network.

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The Chinese VLBI Network (CVN) has stations located in Shanghai, Beijing, Kunming, and Urumqi as well as a VLBI Center in Shanghai that processes four-station data in real time. For the Chang'E-1 project a Mark IV hardware correlator [1] and for the Chang'E-2 project a Mark 5B hardware correlator [2], both shown in Figure 2, were used to process four-station data in real time.

Fig. 2 Chang'E-1 and Chang'E-2 hardware correlators.

2 Chang'E-3 Hardware Correlator

In the recent Chang'E-3 mission, the Chang'E-3 hardware correlator has been used and has performed well. The hardware correlator includes five FPGA boards. All of the FPGA boards have the same hardware: one Xilinx Virtex-4 FX60 and four LX160 FPGAs.

The FX60 FPGA includes a 1-Gigabit Ethernet port and embedded two PowerPC405 processors to send

and receive processing data and control information to and from the outside network.

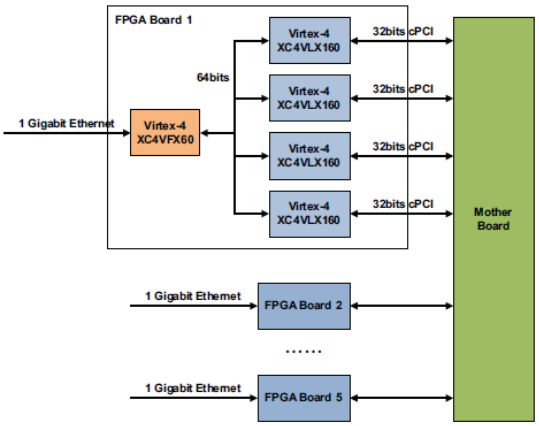

Fig. 3 Diagram of the Chang'E-3 hardware correlator.

The FX60 also connects to four LX160 FPGAs via a 64-bit bus to send and receive processing data and control information to and from each LX160 FPGA. Each LX160 FPGA has a 32-bit cPCI bus connected to the mother board, which connects all five FPGA boards. The FPGA board and the correlator picture are shown in Figure 4.

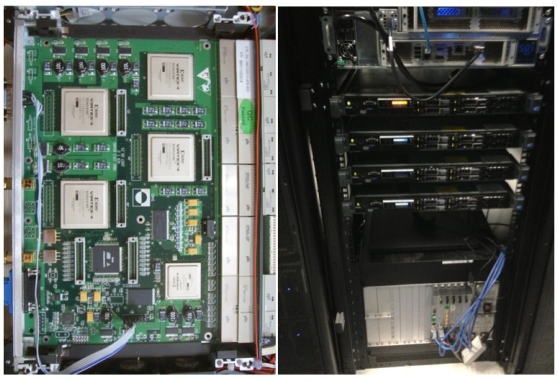

Fig. 4 Chang'E-3 hardware correlator.

3 Results from the Chang'E-3 Mission

Figure 5 shows a comparison between the results of Delta-DOR observations correlated via a hardware correlator and a software correlator. The red points show the results from the hardware correlator, and the black points show the results from the software correlator. Please see the on-line pdf version of this paper to compare the red and the black points in detail. The hardware correlator skips the observation data of third radio source, so there is some difference between the hardware and software correlator outputs in the next two satellite scans and back to the same in the following.

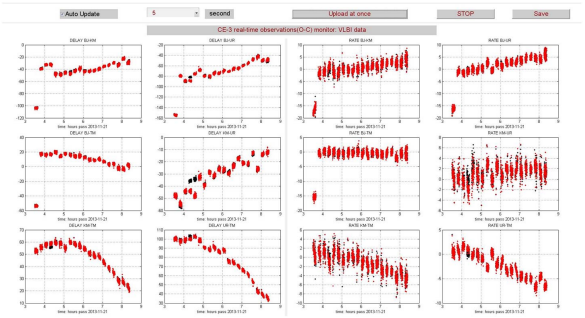

Fig. 5 Comparison between the hardware and software correlators.

Figure 6 shows the final delays from the results sent to Beijing Center from the s3c13a session. The first two scans used the software correlator results, and the following used the hardware correlator results. Between scans two and three there is a small drop, which shows that the hardware correlator delay is about three seconds less than the software correlator delay.

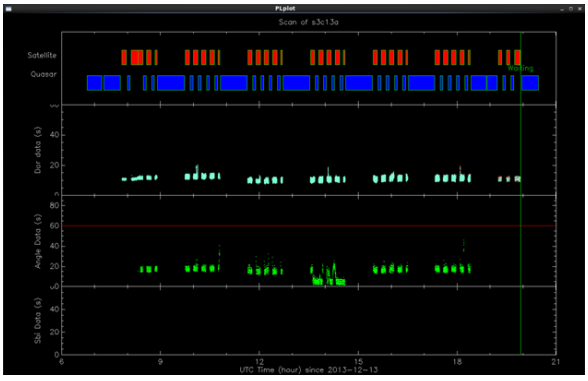

Fig. 6 Hardware and software correlator delays.

4 UniBoard-based Hardware Correlator

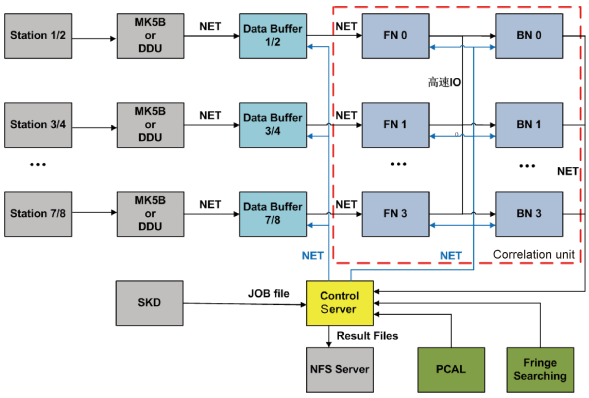

Fig. 7 UniBoard-based hardware correlator.

Currently, we are designing a UniBoard version of the hardware correlator as the next generation correlator. Its features are:

- Outside data are transmitted to a Data Buffer server using the TCP/IP Protocol.
- The Data Buffer server sends data to the Uniboard Front Node via a 10GbE port using the UDP Protocol.
- Data is processed in four Front Nodes and sent to the Back Node via high speed I/O on the Uniboard.
- The results on the Back Node are sent to a PC via a 1GbE port using the TCP/IP Protocol.
- The data is sent to the Front Node via a 10GbE interface.

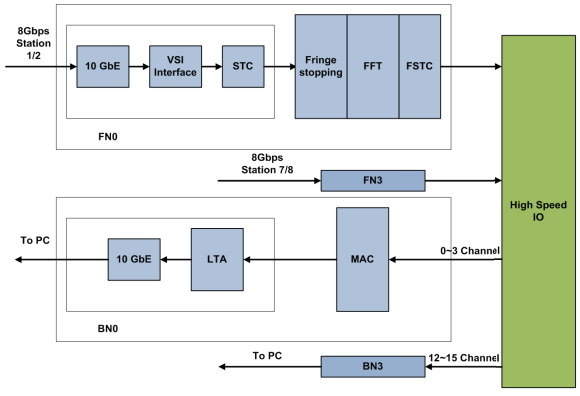

Fig. 8 Diagram of the UniBoard-based hardware correlator.

- The VSI Interface gets the data from the 10GbE interface, then synchronizes and reformats the data.
- The Sample Time Correction (STC) block takes the integer part of the delay model.
- The data is sent for Fringe Stopping using Phase Model coefficients.
- After Fringe Stopping, the data is sent to an FFT, which can be set to between 1,024 and 65,536 FFT points. The output data will be in the natural order.
- Fraction Sample Time Correction (FSTC) uses the fractional part of the delay model.
- Output data is sent to the Back Node FPGA via high speed I/O.
- In the Back Node, data is sent to a Multiply-Accumulate (MAC) unit.
- After the MAC, the data is sent to the Long Term Accumulator (LTA).
- The results are sent to a PC via a 1GbE port using the TCP/IP Protocol.

5 Future Plans

Our future plans include:

- Expansion to an eight-station 32-channel system;
- Update to a single precision floating point FFT and MAC;
- Update to a 10GbE Ethernet;
- Update to a VDIF interface;
- Update to a JIVE UniBoard.

References

1. Xu, Z. J., et al. Real Time Correlator in FPGA. IVS 2006 General Meeting Proceedings, NASA/CP-2006-214140, pp. 89–92.
2. Zhang, X. Z., et al. VLBI Technology Development at SHAO. IVS 2010 General Meeting Proceedings, NASA/CP-2010-215864, pp. 383–387.