Control System and Visualization of the VLBI Hardware Correlator at SHAO

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Abstract The VLBI system is comprised of VLBI stations, data preprocessing, correlator, post-correlator, SKD, orbit, location, and so on. The corrlator processor is the core equipment of the VLBI data preprocessing device; we can calculate important parameters such as the delay, delay rate, correlation amplitude, and interferometric phase from the correlator. Now our group has realized a complete software control system and an FPGA core for the hardware correlator on a CPCI board through the playback interface. We have also achieved the visualization of the processing data for convenience and the C/S architecture for controlling the PBI interface. In the future, our group will port the whole system to the Uniboard board—for speed improvement and supporting more modes. Recently, the real-time mode and post-correlation were tested during the CE-3 mission. The result was also checked to make sure our hardware correlator is fine. This paper describes the whole control system and its realization.

Keywords VLBI, hardware correlator, FPGA, fringe search, Uniboard

1 Introduction

The technique of Very Long Baseline Interferometry (VLBI) has been employed to achieve extremely high angular resolution in the study of radio sources. VLBI has been used in the Chinese Lunar Exploration Program with the participation of the CVN (Chinese VLBI Network) stations. As shown in Figure 1 the Shang-

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hai Astronomical Observatory's VLBI Center includes four VLBI stations (including Shanghai station, Beijing station, Kumming station, and Urumqi station; later to be joined by Sheshan station), data preprocessing, correlator, post-correlator, SKD, orbit, location, and so on.
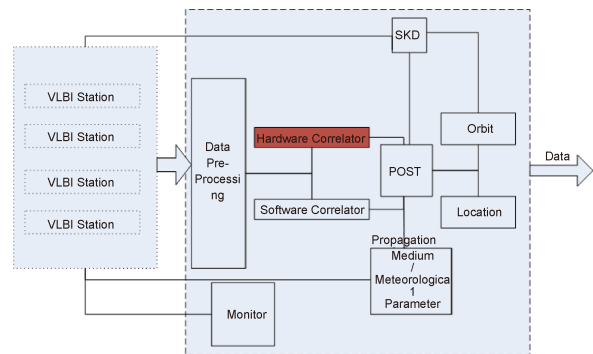

Fig. 1 Diagram of the Chinese VLBI Center.

The hardware correlator is the core equipment of the VLBI data preprocessing device with a complicated high speed processing system. It produces the signal's correlation function and complex visibility function (mutual spectral-density function), from which important parameters can be derived such as the delay, delay rate, correlation amplitude, and interferometric phase. There are two types of correlators; we chose the FX hardware correlator. It completes the data format transition, time synchronization, time-delay compensation, FFT calculation, plural cross-multiplication accumulation, long-term accumulation, and eventually produces the correlation output for post-processing [1].

The Shanghai VLBI Correlator is hosted and operated by the Shanghai Astronomical Observatory, Chi-

nese Academy of Sciences. It is dedicated to the data processing of the Chinese domestic VLBI observing programs, inclusive of the CMONOC project for monitoring the Chinese regional crustal movement and the Chinese deep space exploration project for tracking spacecraft [2].

2 Correlator Procedure

The VLBI correlator is the "glue" that brings the data from separate antennas together and processes it to form the basic observables used in astronomy and geodesy [3]. The correlation procedure goes through the following steps: transfer of observation data from the antenna to the correlator unit through the 10 GbE Internet interface, decoding of the real data to original data by unpacking the frame header information, integer sample time compensation (ISTC), integer sample bit delay compensation, fringe rotation, FFT and fractional sample time compensation (FSTC), transport of the processed data to back-end chips via the high speed serial bus for cross-multiplication in the baseline unit after synchronization, and derivation of the visibility function. The final data are sent to the NFS server in a special data format. The whole system is running under the arrangement of a JOB file. The JOB file contains the following: observed object, observed time, observed frequency, observed bandwidth, observed channels, model, and so on. The hardware correlator also operates by using the JOB file [4].

3 Hardware Correlator System Architecture

Suppose there are two signals f(t) and g(t) as shown in Figure 2. The corresponding FFT transforms are F(w) and G(w).

As we all know, correlators can be grouped into FX and XF types by the sequence of the FFT and multiplication operations. The name "FX" was originated by Chikada (Chikada et al., 1987), who also built the first such correlator, to indicate this reversal of the order of operations compared to the conventional lag correlator. The VLBA correlator group, while considering one
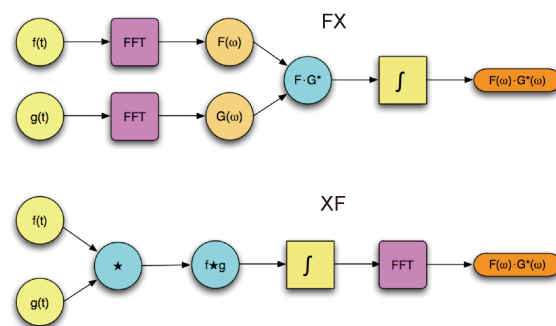

Fig. 2 Equivalence of the FX and XF correlator architectures.

design of each type, adopted the term "XF" which is sometimes used for the latter architecture. Both the FX and the XF correlators include:

- model: delay compensation, fringe rotation
- data sources
- fringe detection & observable parameter estimation
- technical details: discrete samples, integration, correlator beam

There are many advantages of FX; e.g., the cost for the spectral channels grows only with the

$$\log_2(N) \qquad \text{vs.} \qquad N$$

(linear) for XF and there is little loss due to delay quantization.

We chose the FX correlator after taking many factors into consideration. The hardware correlator system includes:

- CCC: center control computer, which controls the whole flow;
- Five FPGA boards: include the core algorithm of the correlator process;
- PBI: the playback interface will playback the raw data to FPGA.

The CCC commuticates with the FPGA through the Peripheral Component Interface (PCI) bus, which is driven by the PCI drive module. As the PCI rate can reach 264 MB/s, which already reaches the command of the current hardware correlator system.

As shown in Figure 3, the PCI bus connects the CCC and the POWERPC (PPC) on the FX60. They access the 64-MB memory at the same time. The PCI interface carries out the definitions and introductions of the memory.
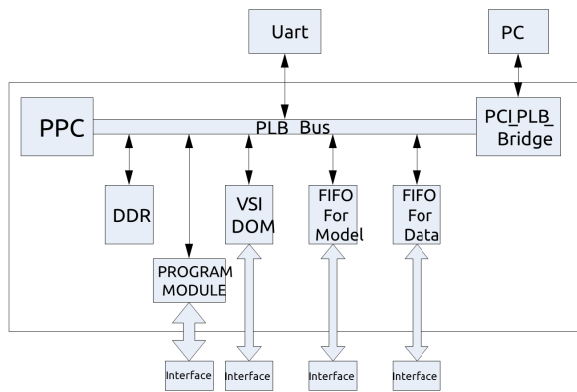
Fig. 3 Hardware correlator system architecture.

Fig. 4 Layout of the hardware correlator.

The CCC sends control commands and parameters to the FX60 to control the relevant FPGA chips, and the status is fed back to the CCC. The concrete functions of the CCC are:

- Load LX160: download the bin file into the FPGA through the PCI bus,
- Initialize FPGA: initialize the FPGA to original status,
- Set parameters: include 50 bytes to control the FPGA,
- Set modules: generate the modules for the correlator,
- Read parameters: feed back the status of FPGA to CCC,
- Record the correlator data: save the correlator data to NFS.

4 Realization of the Hardware Correlator

Figure 4 shows how the CCC connects the PC node and the playback unit (PBU) via the local area network. Thus the CCC can control the PBU by the client/server (C/S) mode, which starts the PBI program automatically. Five FPGA cards connect directly via the network to the PBU.

The playback data is mounted on the NFS, so that the same data can be shared with the software correlator.

A correlator must cross-multiply the signals from different antennas that correspond to the same arriving wave front. But the antennas are at different distances from the source, so th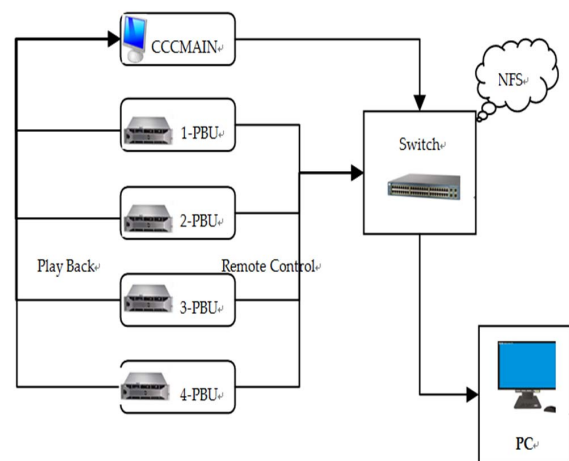e wave front arrives at different times (the delay). Also they are moving at different speeds along the direction to the source, causing different Doppler shifts (the fringe rate). An estimate of these time and rate offsets is removed in the correlator hardware.

5 The Result of Visualization

Figures 5 and 6 are the result of the visualization of the real-time correlator. The magenta (dark gray) lines represent the correlation amplitude and the cyan (light gray) points represent the interferometric phase. The data is the real data from the CE-2 (Chinese Lunar Exploration Program). There are four stations in total. Based on the shared memory technology, we can handle the correlation process and watch the result at the same time. In this way, we can immediately find if there was any error. Also, after using the fringe search technology, the result shows that it has some influence on the delay.

6 Conclusions

It is important to understand that the model we used is never quite accurate; however, it is accurate enough so that the differences between the model and reality are small and are within the search range of the correlator processing. These differences are called the
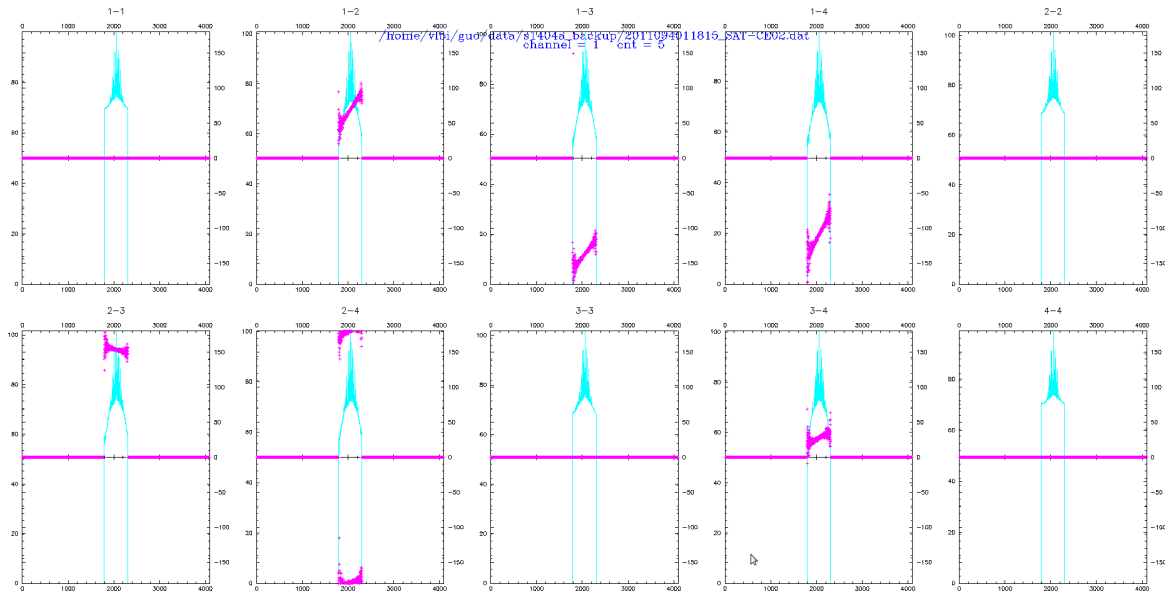
Fig. 5 Result without fringe search. There are four stations involved in the observations, so the figure includes four autocorrelation products and six cross-correlation products. The magenta (dark gray) lines represent the correlation amplitude and the cyan (light gray) points represent the interferometric phase.
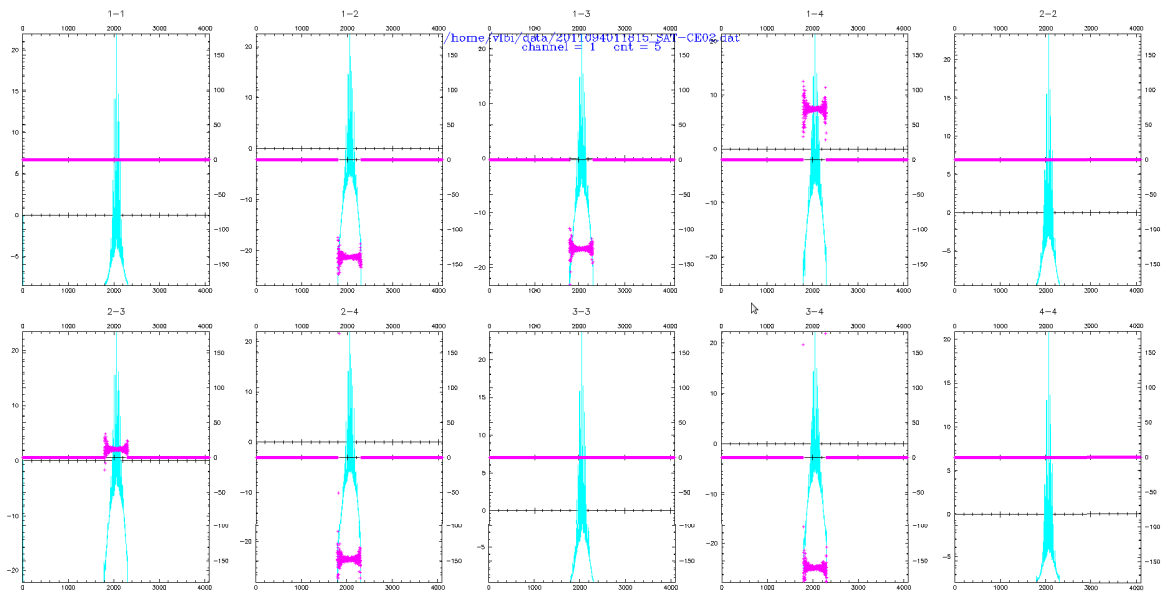
Fig. 6 Result with fringe search. We can see the fringes become flat after the fringe search function, indicating that the residual delay is very low compared to the figure above.

residual differences, or just residuals. In the discussion of single-band and multi-band delay determinations, we are dealing with residuals to the computer model and trying to determine the best estimate delay, delay rate, and phase of these residuals. Once determined, the residuals are added to the original model parameters to arrive at the total observables (e.g., delay, rate, phase) that are used in post-correlation analysis [3].

The usual fringe search technique for VLBI is correlator-based. We can get the conclusion that the result is better when we use the fringe search function.

Of course, this method can solve for motion that is not very intense, but for violent motion we need to further reduce the integration time. This may cause a sharp increase in the amount of data, requiring the algorithm to be optimized further. For future development, we are considering the use of the GPU for the compute-intensive part.

After handling the same data with and without fringe search (Figures 5 and 6), we can see the change of delay and delay rate between the two figures. The result without fringe search has an offset delay of about 200 ns. When using the fringe search module, the delay can be reduced to about 10 ns, which can be ignored for the final result. Here we just modify the delay by the model mentioned before [5]. The tiny change in the trend of the delay rate will be added in the future.

Acknowledgements

References

1. Zhu Renjie, Zhang Xiuzhong, Xiang Ying, Xu Zhijun. An Introduction to the VLBI Correlator Used in the Chinese Lunar Exploration Program. *PROGRESS IN ASTRONOMY*, Vol.26, No.1, pp. 62–72, March 2008.

2. Shu Fengchun, Zheng Weimin, Chen Zhong. IVS 2012 Annual Report *ftp://ivscc.gsfc.nasa.gov/pub/annual-report/2012/pdf/coshao.pdf*

3. Alan R. Whitney. How Do VLBI Correlators Work?, in International VLBI Service for Geodesy and Astrometry 2000 General Meeting Proceedings, edited by Nancy R. Vandenberg and Karen D. Baver, NASA/CP-2000-209893, 2000.

4. Zhang Xiuzhong, Zheng Weimin, Ren Fangbin, Zhu Congxin, Shu Fengchun, Xiang Ying. The High-speed FX Correlator of Chinese VLBI Network? A Super Spectrum Analyzer Based on Programmable ASIC Circuits and Systems, 2000. IEEE APCCAS 2000. The 2000 IEEE Asia-Pacific Conference, pp. 854–858.

5. Shu F. C., Zhang X. Z. The accuracy analysis of model using in correlator process software system, Progress in Astronomy, No. 22, pp. 100–106, 2001.